REEL LCI Database

Methodology Report

Version 0.1

January 12, 2026

Abstract

This report documents the methodology for a Life Cycle Inventory (LCI) database covering a comprehensive range of electronics components. Coverage includes semiconductor integrated circuits across technology nodes from 180nm to 3nm, memory devices (DRAM, NAND flash, HBM), printed circuit boards, passive components (capacitors, resistors, inductors), IC packaging, cables and interconnects, and electromechanical components. The database provides cradle-to-gate inventory data derived exclusively from publicly available sources using a bottom-up "virtual factory" modeling approach. This methodology report follows ISO 14040/14044 guidance and aims to provide LCA practitioners with sufficient information to evaluate data quality, understand allocation procedures, and appropriately apply the inventory data in their assessments.

Version History

This section documents major updates to the methodology report and underlying database.

Table 0.1: Document and database version history

Version	Date	Changes
0.1	TBD	Initial release. 204 component types across 17 categories; 190 process files; elementary flow mapping to ecoinvent v3.12; data quality audit completed; ISO 14040/14044 methodology alignment.

Contents

List of Tables

List of Figures

Chapter 1

Introduction

1.1 Background and Context

Electronics manufacturing represents one of the most complex and environmentally intensive industrial sectors (**williams2002**; **boyd2009**). As semiconductor process complexity increases with each technology node, manufacturing energy intensity continues to grow; imec estimates that IC manufacturing could account for 3% of total greenhouse gas emissions by 2040 (**imec_sustainability2024**). Meanwhile, data centers consumed approximately 1.5% of global electricity in 2024, a figure projected to double by 2030 driven largely by AI workloads (**iea_energy_ai2025**). This growth underscores the importance of understanding embodied carbon in electronics, as hardware manufacturing impacts may rival or exceed operational energy use for certain IT equipment. Despite this significance, the sector suffers from a lack of openly available life cycle inventory (LCI) data. This data gap presents substantial challenges for:

- **Corporate sustainability teams** attempting Scope 3 emissions accounting for purchased electronics
- **Product designers** seeking to make informed eco-design decisions
- **LCA practitioners** conducting assessments of electronics-containing products
- **Policy makers** developing environmental regulations for the electronics sector

1.1.1 The Electronics Data Challenge

Existing LCI data for electronics is limited by several factors:

Proprietary barriers Semiconductor manufacturers treat process data as highly confidential competitive intelligence. Direct measurement data from operating fabrication facilities is rarely shared publicly.

Rapid technology evolution Moore's Law scaling means that manufacturing processes evolve on 2–3 year cycles, making older data quickly obsolete for advanced technology nodes (**irds2024**).

Supply chain complexity A single semiconductor product may involve 10+ distinct manufacturing facilities across multiple countries, making data collection extremely challenging.

Aggregation obscures detail When companies do report environmental data, it is typically aggregated at the facility or company level, obscuring the process-level detail needed for product LCA.

1.1.2 Project Mission

The REEL LCI Database addresses these challenges through a bottom-up "virtual factory" modeling approach that constructs detailed, auditable inventory data using only publicly available information. Rather than relying on proprietary facility measurements, this approach synthesizes data from:

- Equipment vendor technical specifications
- Peer-reviewed academic literature
- Corporate sustainability reports and disclosures
- Industry standards and technology roadmaps
- Patent filings with process parameters
- Engineering calculations based on physics and chemistry

This public data policy ensures that all values in the database are fully traceable to documented sources, enabling independent verification and continuous improvement by the user community.

1.2 Goal and Scope

1.2.1 Database Goal

The goal of this database is to provide openly documented, estimated life cycle inventory data for electronics components, enabling practitioners to conduct cradle-to-gate environmental assessments without requiring access to proprietary manufacturing data.

The database produces **inventory data only**: the quantified inputs and outputs associated with manufacturing processes. This includes energy consumption (electricity, natural gas, steam), water use (ultrapure water, process water, cooling water), material inputs (chemicals, gases, metals, substrates), wastewater generation, and air emissions (including greenhouse gases and volatile organic compounds). The database does not provide characterized impact results (such as kg CO_2e or kg SO_2e), as these require user selection of appropriate impact assessment methods.

1.2.2 Temporal and Geographical Scope

Temporal Scope

The database represents the manufacturing landscape as of **2023–2025**. Process parameters, equipment specifications, and facility characteristics reflect current production practices for each technology node. Given the rapid evolution of semiconductor manufacturing, users should consider temporal relevance when applying this data:

- **Advanced nodes** (3nm–7nm): Data reflects 2023–2025 production ramp characteristics
- **Mature nodes** (14nm–65nm): Data reflects established high-volume manufacturing
- **Legacy nodes** (90nm+): Data reflects mature, stable processes

Geographical Scope

The virtual factory models represent **global average** manufacturing practices rather than region-specific facilities. However, certain parameters have significant regional variation that users must address:

Electricity grid mix The database provides electricity consumption as a separate flow. Users must link to appropriate regional grid mix data for their specific supply chain geography (see Chapter 5 for guidance).

Default geography assumptions When regional data is required for modeling, the following defaults apply: advanced logic (Taiwan), memory (South Korea/Taiwan), packaging (Asia-Pacific average), PCBs (China/Taiwan).

Electricity grid mix is typically the single most sensitive parameter for climate impact calculations. Users with known supply chain geography should substitute appropriate regional electricity data.

1.2.3 Reference Flows

Following ISO 14044 terminology, the database uses **reference flows** rather than functional units for these intermediate products. A capacitor or semiconductor die does not have an intrinsic function until integrated into a final product; however, it has a defined reference flow (e.g., one piece, one wafer) that serves as the basis for inventory calculations.

Table 1.1: Reference flows by component category

Category	Reference Flow	Notes
Semiconductor wafers	per wafer	300mm diameter; 200mm available for legacy nodes
Semiconductor dies	per die, per cm^2	Yield allocation: all burdens assigned to good dies; defective dies treated as process waste
Complete ICs	per IC	Combines wafer + packaging
Memory components	per component	HBM stacks, DRAM ICs
PCBs	per m^2	Normalized to board area
Passive components	per piece, per 1000 pieces	MLCCs, resistors, inductors
Packaging	per package	Various package types
Cables	per meter	Cable assemblies

1.2.4 Intended Applications

The database is designed to support the following use cases:

Scope 3 emissions accounting Companies can use component-level inventory data to estimate Category 1 (purchased goods) emissions for electronics procurement.

Product LCA LCA practitioners can integrate electronics component data into broader product assessments, linking to background databases for upstream material production.

Eco-design decisions Product designers can compare environmental profiles of alternative components (e.g., different technology nodes, package types, or passive component materials).

Hotspot identification Organizations can identify the most environmentally intensive components in their bill of materials for prioritized improvement efforts.

Scenario analysis Users can model different manufacturing scenarios (e.g., regional grid mixes, abatement technologies) to understand sensitivity to key parameters.

1.2.5 Target Audience

This database and methodology report are intended for:

- LCA practitioners with general knowledge of life cycle assessment but not necessarily semiconductor manufacturing expertise
- Corporate sustainability professionals conducting supply chain assessments
- Product designers evaluating environmental implications of component selection
- Researchers studying electronics manufacturing environmental impacts

1.3 Alignment with ISO Standards

This methodology report is developed following the principles and framework of ISO 14040:2006 (**iso14040**) and ISO 14044:2006 (**iso14044**).

Important clarification: This statement describes alignment with ISO principles and structure, not a formal compliance declaration. Full ISO compliance requires external critical review and specific procedural requirements that depend on the intended application. Per ISO 14044, external critical review is required for any LCA results intended for public disclosure. Users should arrange appropriate critical review when publicly communicating results derived from this database.

The methodology addresses the key elements specified by ISO 14044 for LCI studies:

- **Goal and scope definition** (this chapter)
- **System boundary specification** (Chapter 2)
- **Allocation procedures** (Chapter 2)
- **Data quality requirements** (Chapter 3)
- **Calculation methods** (Chapters 2 and 4)
- **Limitations documentation** (Chapter 6)

1.4 Database Coverage

The database covers **204 distinct component and product types** organized into 14 categories. Table 1.2 summarizes coverage by category.

For products with multiple specifications (e.g., PCB surface finishes, cable lengths), the database provides separate LCI datasets for each variant. In total, the database includes approximately **350–400 distinct LCI datasets**.

Table 1.2: Database coverage by component category

Category	Types	Example Products
Semiconductor wafers	43	3nm–180nm logic, DRAM, NAND, III-V
Complete ICs	17	CPUs, GPUs, HBM, MCUs
PCBs	19	Server, networking, HDI, flex
Passive components	21	MLCCs, resistors, inductors
Cables & connectors	18	DAC, fiber, USB4, power cords
Packaging	30	FC-BGA, QFN, WLCSP
Thermal management	5	Heat pipes, vapor chambers
Optoelectronics	10	Transceivers, LEDs
Specialty semiconductors	20	SiC, GaN, MEMS, CIS
Other	21	Infrastructure, substrates
Total	**204**	

1.5 Report Structure

This methodology report is organized as follows:

Chapter 2: General Methodology describes the core methodological principles including system boundaries, the virtual factory concept, allocation procedures, and data sourcing hierarchy.

Chapter 3: Data Quality and Uncertainty presents the data quality assessment framework, uncertainty characterization methods, and validation approach.

Chapter 4: Sector-Specific Modeling details the modeling approaches for each component category, including technology-specific parameters and key assumptions.

Chapter 5: User Guidance provides practical instructions for integrating the database with background databases and impact assessment methods.

Chapter 6: Limitations and Future Work documents known data gaps, limitations, and planned improvements.

Appendix A: Glossary defines technical terms used throughout the report.

Appendix B: Process Inventory lists all process files in the database.

Appendix C: Data Sources provides the complete list of data sources referenced.

Chapter 2

General Methodology

This chapter describes the core methodological principles underlying the REEL LCI Database, including system boundaries, the virtual factory modeling approach, allocation procedures, and data sourcing hierarchy.

2.1 System Boundaries

2.1.1 Cradle-to-Gate Scope

The database provides cradle-to-gate life cycle inventory data, encompassing:

- **Upstream processes**: Raw material extraction and refinement (via background database linkage)
- **Manufacturing processes**: Component fabrication, assembly, and testing
- **Gate boundary**: Finished component ready for integration into higher-level assemblies

Excluded from scope:

- Use phase (product operation)
- End-of-life treatment (recycling, disposal)
- Distribution and retail
- Inbound transportation of raw materials to the manufacturing facility (included in upstream "market for" datasets when users link to background databases)

Figure 2.1 illustrates the system boundary for semiconductor wafer fabrication, showing the relationship between utility inputs, support processes, process equipment, and outputs.

2.1.2 Treatment of Capital Goods

Capital goods (including manufacturing equipment, cleanroom construction, and facility infrastructure) are currently **excluded** from the system boundary. This exclusion is based on:

- Lack of publicly available data on equipment embodied energy
- Significant uncertainty in equipment lifetime and allocation
- Common practice in electronics LCA to exclude capital goods
- Focus on operational inventory which dominates life cycle impacts

Future versions may include capital goods allocation when sufficient public data becomes available.

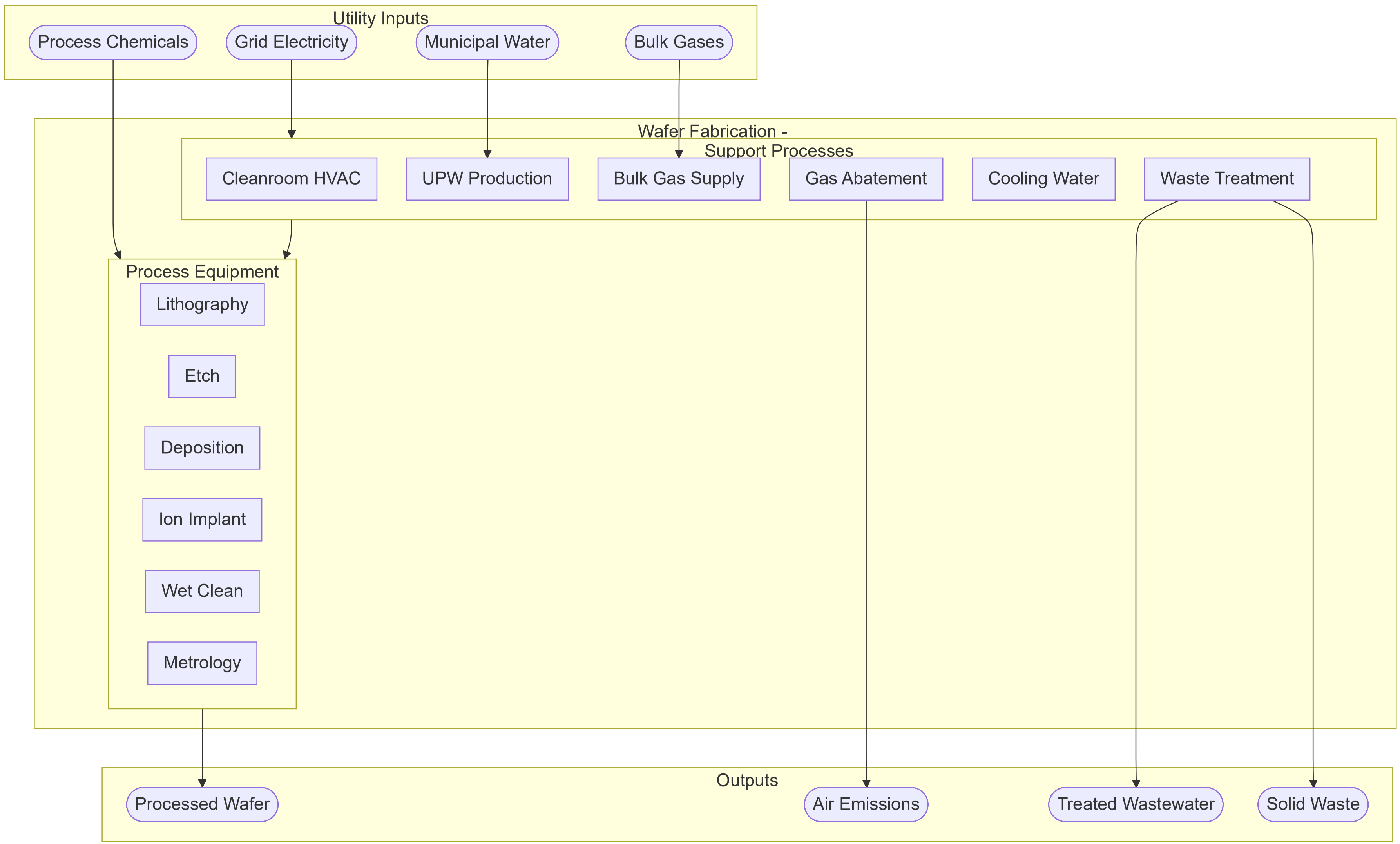

Figure 2.1: System boundary for semiconductor wafer fabrication. Utility inputs (electricity, water, gases, chemicals) flow through support processes and process equipment to produce processed wafers along with air emissions, wastewater, and solid waste. Support processes provide the facility infrastructure required by process equipment.

2.2 Modeling Framework

2.2.1 Attributional Approach

The database follows an attributional modeling approach, quantifying the physical flows directly associated with producing a defined functional unit. This approach:

- Describes the environmentally relevant inputs and outputs of a product system
- Uses average data for processes with multiple suppliers
- Does not model market-mediated effects or consequential changes

2.2.2 Virtual Factory Concept

A **virtual factory** is a modeled representation of manufacturing processes constructed using a bottom-up approach from fundamental process parameters, rather than top-down allocation from facility-level measurements (**murphy2003**; **krishnan2008**). Unlike traditional LCI approaches that rely on primary data collected from specific production sites, the virtual factory builds process inventories from first principles.

This bottom-up methodology is distinguished by:

Process-level granularity Each manufacturing step is modeled individually based on the physics and chemistry of the operation, enabling detailed understanding of inventory drivers.

Equipment-based calculations Energy and material consumption are derived from equipment specifications (power ratings, throughput, gas flows) rather than aggregated facility measurements.

Stoichiometric foundations Chemical consumption is calculated from reaction stoichiometry, film thickness targets, and utilization efficiencies rather than empirical facility averages.

Explicit assumptions All modeling assumptions are documented, enabling users to understand and, where appropriate, modify parameters for their specific context.

The virtual factory approach constructs process inventories from:

1. **Equipment specifications**: Power ratings, throughput, process parameters from vendor documentation
2. **Reaction stoichiometry**: Chemical consumption calculated from balanced equations and target film compositions
3. **Geometric parameters**: Material requirements derived from film thickness, wafer area, and feature dimensions
4. **Utilization factors**: Chamber efficiency, precursor incorporation rates, and waste generation based on published literature

This approach produces models that are independent of any specific facility, representing a generic manufacturing process that can be adapted through parameter adjustments for different scenarios.

2.2.3 Three-Tier Architecture

The calculation system uses a modular three-tier architecture that separates concerns and enables independent updates:

Model files Define *what* to calculate: process flow sequences, pass counts, yield parameters

Configuration files Define *parameters*: facility assumptions, abatement scenarios, support rates

Process files Define *how much*: per-operation energy, materials, emissions

2.3 Cut-off Criteria

2.3.1 Mass and Energy Thresholds

Flows are excluded from process inventories when they contribute less than 1% of the **total mass of inputs to the unit process** or less than 1% of the **total energy input to the unit process**, unless they:

- Involve substances of high environmental concern
- Are specifically regulated (e.g., PFCs, heavy metals)
- Have disproportionate impact potential (e.g., high GWP gases)

Note that the denominator is total process inputs, not product mass. In semiconductor manufacturing, input mass (water, chemicals, gases) is orders of magnitude higher than product mass, so this threshold excludes only truly minor flows.

2.3.2 Toxic Substance Exceptions

The following substance categories are always included regardless of mass contribution:

Table 2.1: Substances included regardless of cut-off criteria

Category	Examples	Rationale
Perfluorocarbons	CF_4, C_2F_6, SF_6, NF_3	GWP 7,000–23,000 (**ipcc_ar6**); EPA regulated
Heavy metals	Pb, Cd, Hg, Cr(VI)	RoHS regulated; high toxicity
Volatile organics	Photoresist solvents, PGMEA	Air quality concerns
Precious metals	Au, Ag, Pd, Pt	High embodied impacts
Ozone depleting	CFCs, HCFCs (legacy)	Montreal Protocol

2.4 Allocation Rules

2.4.1 Process Yield Allocation

Process yields directly affect inventory allocation. For semiconductor manufacturing:

$$I_{\text{per good die}} = \frac{I_{\text{per wafer}}}{Y_{\text{line}} \times N_{\text{geometric}} \times Y_{\text{die}}} \tag{2.1}$$

Where:

I Inventory (energy, materials, emissions)
Y_{line} Line yield (fraction of wafers completing all process steps)
$N_{\text{geometric}}$ Geometric dies per wafer (based on die size and wafer diameter)
Y_{die} Die yield (fraction of dies passing electrical test)

2.4.2 Die Yield Model

Die yield follows the Poisson defect model:

$$Y_{\text{die}} = e^{-D_0 \times A_{\text{die}}} \tag{2.2}$$

Where D_0 is the defect density ($1/\text{cm}^2$) and A_{die} is die area (cm^2).

2.4.3 Multi-Output Process Handling

Multi-output processes are rare in electronics manufacturing. When they occur, the following allocation hierarchy applies:

1. **Physical causation**: Where outputs can be physically assigned to specific inputs (preferred)
2. **Mass allocation**: Proportional to output mass (for similar co-products)
3. **Economic allocation**: Proportional to economic value (last resort)

Current applications:

- **Bin yield**: Lower-performance IC grades receive equal inventory per unit as higher grades (no allocation by grade)
- **Scrap recovery**: Precious metal recovery credits are excluded pending data availability
- **Wafer reclaim**: Excluded; test wafers and scrap are outside system boundary

2.5 Data Sources Hierarchy

The database uses a tiered hierarchy of public data sources:

Table 2.2: Data source hierarchy by reliability

Tier	Source Type	Description
1	Equipment specifications	Vendor datasheets with power, throughput, process parameters
2	Peer-reviewed literature	Academic papers with measured process data
3	Industry roadmaps	IRDS/ITRS public portions
4	Corporate reports	Sustainability reports, investor disclosures
5	Patents	Process descriptions with operational parameters
6	Engineering estimates	Calculated from first principles with documented assumptions

2.5.1 Source Documentation

Every data value in the database includes:

- Source citation with URL where applicable
- Extraction date
- Data quality indicators (see Chapter 3)
- Uncertainty bounds (min/typical/max)

2.6 Calculation Methods

2.6.1 Equipment-Based Energy Calculation

For equipment-limited processes, energy consumption is calculated from:

$$E_{\text{per wafer}} = P_{\text{equipment}} \times t_{\text{process}} = \frac{P_{\text{equipment}}}{\text{Throughput}} \tag{2.3}$$

Where $P_{\text{equipment}}$ represents the **time-weighted average power consumption** (kW) accounting for the duty cycle between active processing, idle, and standby states. Throughput is the effective wafers per hour achieved under normal production conditions. This formulation implicitly captures the operating state mix for a fully utilized fab; users modeling specific scenarios with different utilization rates should adjust accordingly.

Example: EUV lithography

- Power consumption: $1{,}000\,\mathrm{kW}$
- Throughput: 150 wafers/hour
- Energy per wafer: $1000 \times (1/150) = 6.67\,\mathrm{kW \cdot h/wafer}$

2.6.2 Stoichiometric Material Calculation

For chemical processes, precursor consumption is derived from:

$$M_{\text{precursor}} = \frac{M_{\text{film}}}{\eta \times r_{\text{MW}}} \tag{2.4}$$

Where:

$M_{\textbf{film}}$ Deposited film mass (from thickness × area × density)
η Utilization efficiency (fraction incorporated into film, typically 10–50%)
$r_{\textbf{MW}}$ Molecular weight ratio (target element / precursor)

2.6.3 Aggregation to Component Level

Process step inventories are aggregated to component level:

$$I_{\text{per wafer}} = \sum_{s} (I_s \times n_s) \times \frac{1}{Y_{\text{line}}} + I_{\text{support}} \quad (2.5)$$

$$I_{\text{per die}} = \frac{I_{\text{per wafer}}}{N_{\text{geometric}} \times Y_{\text{die}}} \quad (2.6)$$

$$I_{\text{per cm}^2} = \frac{I_{\text{per wafer}}}{A_{\text{wafer}}} \quad (2.7)$$

Where I_s is per-pass inventory for step s, n_s is the number of passes, and I_{support} is allocated facility overhead.

For complete integrated circuits, the aggregation combines wafer fabrication and packaging inventories, applying yield allocation at each stage. Figure 2.2 illustrates this hierarchical aggregation from raw materials through to the finished IC.

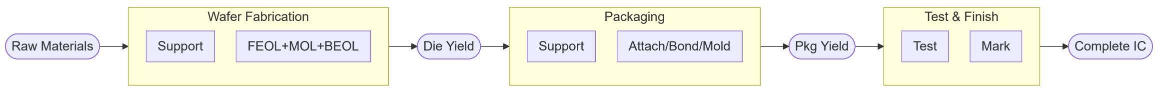

Figure 2.2: Aggregation of inventory for a complete integrated circuit. Wafer fabrication inventory is allocated per die based on die yield, then combined with packaging inventory (allocated by package yield) and test/finish operations to produce the complete IC inventory.

2.6.4 Support Process Allocation

Manufacturing facilities require support processes beyond the direct production equipment. The approach to allocating these support process burdens varies by facility type and production context.

Semiconductor Fabrication Facilities

For semiconductor wafer fabs, facility overhead is allocated per wafer based on fab-wide energy consumption divided by production throughput. Support processes for fabs include:

Cleanroom HVAC Fan filter units (FFUs), makeup air handling, exhaust systems, and temperature/humidity control for cleanroom environments (ISO Class 1–5).

Ultrapure water (UPW) Reverse osmosis, electrodeionization, UV treatment, and polishing systems to produce 18.2 MΩ·cm water required for wafer processing.

Cooling water systems Chillers, cooling towers, and heat exchangers for process tool cooling and facility climate control.

Gas abatement Point-of-use thermal oxidizers, plasma abatement, and wet scrubbers for treating process exhaust streams.

Bulk gas supply On-site generation or delivery of nitrogen, argon, oxygen, and compressed dry air.

Waste treatment Wastewater treatment systems for acids, bases, metals, and fluorinated compounds; solid waste handling.

Water terminology: Following ISO 14046 conventions (**iso14046**), the database distinguishes between water *withdrawal* (gross intake from the source) and water *consumption* (water not returned to the original watershed, primarily evaporative losses from cooling towers and scrubbers). Water that becomes wastewater is classified as *discharge*, not consumption, since it returns to the hydrological system after treatment. The database tracks both withdrawal and consumption metrics.

For advanced logic fabs, support processes typically account for approximately 70% of total facility energy consumption, with the remainder consumed by process equipment. Figure 2.3 shows the breakdown of support process energy for a representative 7nm logic fab.

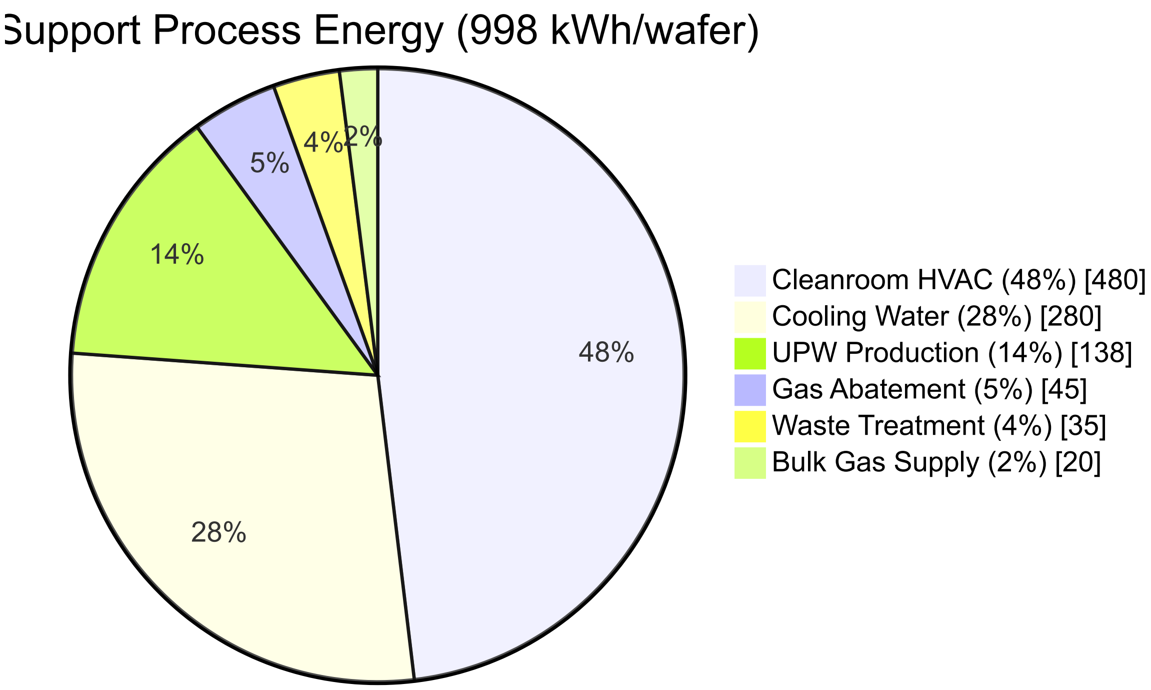

Figure 2.3: Breakdown of support process energy consumption for advanced logic wafer fabrication (7nm example). Cleanroom HVAC dominates at approximately 48% of support energy, followed by cooling water systems and ultrapure water production.

PCB Manufacturing Facilities

PCB facilities operate without cleanroom requirements and have different support process profiles. Key support processes include:

Process water treatment Deionized water for rinse tanks, typically lower purity than semiconductor UPW.

Wastewater treatment Significant treatment requirements for copper-laden rinse water, spent etchants, and plating bath effluents.

Fume extraction Local exhaust ventilation for etch, plating, and lamination processes.

Compressed air For pneumatic equipment and process applications.

Support energy for PCBs is allocated per square meter of board produced.

Passive Component Manufacturing

Passive component facilities (MLCCs, resistors, inductors) have support requirements that vary significantly by product type:

Sintering furnaces High-temperature kilns dominate energy consumption for ceramic components.

Controlled atmospheres Nitrogen or nitrogen/hydrogen atmospheres for sintering and soldering.

Plating systems Electroplating for terminations with associated water treatment.

Support energy for passives is allocated per piece or per kilogram of product depending on the component type.

Packaging and Assembly Facilities

OSAT (Outsourced Semiconductor Assembly and Test) facilities have intermediate requirements between wafer fabs and PCB facilities:

Cleanroom (reduced) Class 100–10,000 cleanrooms for die attach and wire bonding; less stringent than wafer fabs.

Cooling water For molding equipment and test systems.

Compressed air Pneumatic handling and packaging equipment.

No PFC abatement is required as packaging processes do not use fluorinated etch or clean gases.

Production Facility Assumptions

Support process burdens are allocated based on reference facility parameters. Table 2.3 documents the production capacity assumptions used for different facility types.

Table 2.3: Reference facility parameters for support process allocation

Facility Type	Capacity	Support Energy	Wafer Size
Advanced logic (3–7nm)	50,000 wpm	998 kWh/wafer	300mm
Mature logic (28nm+)	80,000 wpm	350 kWh/wafer	300mm
Memory (DRAM/NAND)	100,000 wpm	650 kWh/wafer	300mm
Legacy logic (130nm+)	30,000 wpm	200 kWh/wafer	200mm

These parameters represent typical high-volume manufacturing facilities operating at steady-state production. Support energy scales non-linearly with capacity; facilities with higher throughput achieve better per-wafer efficiency due to economies of scale in HVAC and utility systems.

Note on utilization: Real fabrication facilities operate at less than 100% of rated capacity due to equipment maintenance, changeovers, and demand fluctuations. The support energy values above represent the per-wafer burden under steady-state production conditions. Lower utilization does not change the per-wafer inventory; it simply means fewer wafers are produced annually, with facility overhead allocated across actual production output. Users modeling specific facilities should use the same per-wafer values regardless of utilization rate.

2.7 Custom Upstream Material Datasets

Several semiconductor-specific materials are not available in standard LCI databases such as ecoinvent. For these materials, the REEL database provides custom upstream datasets with full gate-to-gate inventories. These datasets enable complete supply chain tracing for specialty process chemicals.

2.7.1 Materials Covered

Table 5.1 lists the custom upstream material datasets included in the database.

Table 2.4: Custom upstream material datasets

Material	Formula	Use in Semiconductor Manufacturing
Nitrogen trifluoride	NF_3	CVD/PVD chamber cleaning gas
Octafluorocyclobutane	C_4F_8	Oxide/nitride etch gas
Hexafluoro-1,3-butadiene	C_4F_6	High-aspect-ratio etch gas
Tungsten hexafluoride	WF_6	Tungsten CVD precursor
Elemental fluorine	F_2	Remote plasma chamber clean, base for F-gases
ArF photoresist	(mixture)	193nm DUV lithography
PGMEA	$C_6H_{12}O_3$	Photoresist solvent
TMAH	$(CH_3)_4NOH$	Photoresist developer
CMP slurries	(mixtures)	Oxide, copper, tungsten planarization

2.7.2 Methodology for Custom Datasets

Each upstream material dataset follows a consistent methodology:

1. **Stoichiometric calculation**: Material inputs are derived from balanced chemical equations for the primary production route.
2. **Literature energy values**: Process energy is sourced from academic literature, patents, or engineering estimates based on thermodynamic requirements.
3. **ecoinvent linkage**: Where possible, input materials reference ecoinvent datasets. Materials not in ecoinvent are either proxied to similar compounds or linked to other custom datasets.
4. **Yield adjustment**: Production yields (typically 70–95%) account for byproduct formation and process losses.

2.7.3 Data Quality Considerations

These custom datasets have lower data quality than ecoinvent datasets due to reliance on calculated values rather than measured plant data. Key limitations include:

- Energy values are often theoretical minimums or engineering estimates rather than measured industrial consumption
- Proprietary formulations (especially for photoresists and CMP slurries) require proxy compositions

- Regional variation in production processes is not captured

Users requiring higher fidelity upstream data should consult specialty chemical manufacturers directly or commission facility-specific studies.

Chapter 3

Data Quality and Uncertainty

This chapter describes the data quality assessment framework and uncertainty characterization methods used throughout the database.

3.1 Data Quality Indicators

3.1.1 Modified Pedigree Matrix

Data quality is assessed using a modified pedigree matrix adapted for virtual factory modeling (**weidema2013**; **ciroth2016**). Unlike traditional LCI databases that can verify primary data collection, this database relies on secondary public data, requiring adapted quality criteria.

Table 3.1: Data quality indicator dimensions

Dimension	Description
Reliability	Quality of the underlying measurement or calculation method
Completeness	Representativeness of the sample for the intended scope
Temporal	Currency of the data relative to technology evolution
Geographic	Alignment with major production regions
Technological	Specificity to the exact process or technology

3.1.2 Scoring Criteria

Each dimension is scored on a 1–5 scale (1 = best quality):

Reliability

Score	Criteria
1	Verified process data from peer-reviewed literature or detailed vendor specifications
2	Calculated from well-documented equipment specifications and stoichiometry
3	Calculated from theoretical physics with reasonable assumptions
4	Extrapolated from related processes or older technology nodes
5	Rough engineering estimate or rule of thumb

Completeness

Score	Criteria
1	Data covers all known process steps and flows >1% of mass/energy
2	Major process steps covered; minor flows estimated
3	Covers major energy consumers; minor chemical flows estimated
4	Partial coverage; significant flows estimated or missing
5	Representative proxy only; substantial uncertainty

Temporal Correlation

Score	Criteria
1	Data/specification <3 years old
2	Data 3–5 years old
3	Data 5–7 years old
4	Data 7–10 years old
5	Data >10 years old (significant for Moore's Law technologies)

Geographic Correlation

Score	Criteria
1	Specific to major production region (Taiwan, South Korea, US, EU)
2	Global average representing production-weighted mix
3	Proxy region used with grid/efficiency adjustment
4	Unspecified region; assumed global average
5	Unknown geography; potential significant variance

Technological Correlation

Score	Criteria
1	Exact match to technology node/process type
2	Adjacent node data with documented scaling
3	Similar technology class used as proxy
4	Related technology with significant assumptions
5	Different technology class used as proxy

3.1.3 Composite DQI Reporting

Data quality indicators are reported as a **vector of individual scores** (R, C, T, G, Te) to preserve transparency, along with a **geometric mean** as the summary indicator:

$$\text{DQI}_{\text{summary}} = \sqrt[5]{R \times C \times T \times G \times Te} \quad (3.1)$$

Where R = Reliability, C = Completeness, T = Temporal, G = Geographic, Te = Technological.

The geometric mean provides a balanced summary that is sensitive to poor scores in any dimension while avoiding the extreme conservatism of using the maximum. For example, data that is verified (R=1) but from a different technology class (Te=5) with other dimensions at 2 would receive a summary DQI of $\sqrt[5]{1 \times 2 \times 2 \times 2 \times 5} \approx 2.1$, indicating acceptable quality with caution advised.

Note: The DQI is **purely qualitative metadata** for user assessment. It is not computationally linked to the quantitative min/typical/max uncertainty bounds, which are determined independently based on source documentation and engineering judgment.

Table 3.2: DQI interpretation guide

DQI Score	Interpretation
1	High quality; suitable for detailed assessments
2	Acceptable quality; appropriate for most applications
3	Use with caution; consider sensitivity analysis
4–5	Screening quality only; significant uncertainty

3.2 Uncertainty Characterization

3.2.1 Min/Typical/Max Representation

All quantitative data in the database is characterized using three-point estimates:

Minimum Lower bound based on best-case assumptions or lowest reported values
Typical Central estimate representing expected or most common values
Maximum Upper bound based on worst-case assumptions or highest reported values

This representation captures both:

- **Variability**: Real differences between facilities, equipment generations, operating conditions
- **Uncertainty**: Lack of precise data requiring estimation

3.2.2 Variability vs. Uncertainty

The database distinguishes between:

Variability (aleatory uncertainty):

- Inherent differences between fabs, equipment, operating conditions
- Cannot be reduced with more data; reflects real-world variation
- Example: Energy consumption varies 15–25% across fabs at same node

Uncertainty (epistemic uncertainty):

- Lack of precise measurement or complete information
- Can be reduced with better data or more detailed models

- Example: Gas utilization efficiency not reported; estimated from physics

3.3 Uncertainty Propagation

3.3.1 Interval Arithmetic Approach

The calculation engine propagates uncertainty using interval arithmetic:

$$[a, b] + [c, d] = [a + c, b + d] \tag{3.2}$$

$$[a, b] \times [c, d] = [\min(ac, ad, bc, bd), \max(ac, ad, bc, bd)] \tag{3.3}$$

For positive intervals (typical in LCI):

$$[a, b] \times [c, d] = [a \times c, b \times d] \quad \text{where } a, c > 0 \tag{3.4}$$

Important limitation: Interval arithmetic is computationally simple but produces **theoretical worst-case bounds**, not probability distributions. When aggregating many process steps (as in semiconductor manufacturing with hundreds of steps), interval bounds expand conservatively and may be wider than would be observed in practice. Users requiring probabilistic uncertainty estimates should apply Monte Carlo sampling to the min/typical/max values using triangular distributions.

3.3.2 Implementation

The `UncertainValue` class implements:

- Addition, subtraction with interval bounds
- Multiplication, division with bound propagation
- Aggregation across process steps
- Yield-adjusted allocation

Example: Aggregating two process steps with uncertainty:

$$\text{Step 1 energy} = [5.0, 6.0, 8.0] \text{ kWh (min/typ/max)}$$
$$\text{Step 2 energy} = [3.0, 4.0, 5.0] \text{ kWh}$$
$$\text{Total energy} = [5.0 + 3.0, 6.0 + 4.0, 8.0 + 5.0] = [8.0, 10.0, 13.0] \text{ kWh}$$

3.3.3 Priority Flows for Robust Modeling

Detailed uncertainty modeling focuses on flows that typically dominate environmental profiles in electronics manufacturing. Based on literature review of published electronics LCA studies, the following flow categories warrant the most careful uncertainty characterization:

Electricity consumption Often the largest single contributor to manufacturing environmental footprint when characterized for climate change. Uncertainty in electricity consumption propagates directly to characterized results.

Water consumption Particularly significant for semiconductor manufacturing where ultrapure water production is energy-intensive and water stress varies geographically.

Specialty gases Perfluorocarbons (CF_4, C_2F_6, SF_6) and nitrogen trifluoride (NF_3) have high global warming potentials, making even small mass flows potentially significant.

Precious metals Gold and palladium in packaging have high embodied impacts per unit mass from mining and refining.

Solvents and specialty chemicals Volatile organic compounds in photoresists and cleaning solvents can be significant for air quality impacts.

Flows contributing less than 1% of mass and energy use simplified uncertainty factors unless they involve substances of particular environmental concern.

3.4 Source Documentation Requirements

3.4.1 Required Metadata

Every data value in the database must include the following documentation:

Table 3.3: Required metadata fields for data values

Field	Type	Description
`value`	Numeric	The data value
`unit`	String	Physical unit (SI preferred)
`source_type`	Enum	Category from source taxonomy
`source_title`	String	Document title or publication name
`source_url`	URL	Direct link if publicly available
`source_date`	Date	Publication or measurement date
`extraction_date`	Date	When data was extracted
`page_or_section`	String	Location within source document
`context`	String	Conditions, scope, or caveats

3.4.2 Source Type Taxonomy

Data sources are classified using a standardized taxonomy:

`equipment_spec` Vendor technical documentation, datasheets

`academic_paper` Peer-reviewed journal publications

`conference_paper` Conference proceedings (IEDM, VLSI, ECTC)

`corporate_report` Sustainability reports, annual reports, CDP disclosures

`industry_standard` SEMI, IEEE, or other standards body documents

`patent` Patent filings with technical specifications

`trade_publication` Trade magazines, industry news

`government_report` EPA, DOE, EU JRC publications

`calculated` Derived from other documented data

`estimated` Engineering estimate with documented basis

`assumed` Explicit assumption (requires justification)

3.4.3 Uncertainty Basis Guidelines

Default uncertainty ranges based on source quality:

Table 3.4: Default uncertainty ranges by data situation

Situation	Default Range
Specification states "X ± Y%"	Use stated tolerance
Single source, verified	±25%
Multiple sources agree	Min/max of sources
Multiple sources disagree	Full range, investigate
Engineering estimate	±50% minimum
Scaling from other node	±40% additional
Assumed value	±100% or justify

3.5 Data Gap Management

Data gaps (parameters for which no adequate public data could be found) are an inevitable reality when constructing LCI data from secondary sources. This section documents how gaps are identified, characterized, and addressed through workaround strategies.

3.5.1 Gap Identification Criteria

A data gap is formally documented when any of the following conditions apply:

No public data available Extensive literature search yields no quantitative data for a required inventory parameter.

Temporal inadequacy Available data is older than 10 years for a rapidly evolving technology, making extrapolation to current processes unreliable.

Low reliability Available data has significant quality concerns (e.g., values derived from outdated proxies, missing documentation of measurement conditions).

Applicability uncertainty Data exists but its applicability to the specific process or technology generation is questionable.

3.5.2 Gap Prioritization

Gaps are prioritized based on their potential impact on inventory accuracy:

High priority The parameter affects flows contributing more than 10% of total energy, water, or a key material category. Resolution is essential for model credibility.

Medium priority The parameter affects flows contributing 1–10% of totals. Resolution improves accuracy but models remain usable with documented uncertainty.

Low priority The parameter affects flows contributing less than 1% of totals, or relates to secondary parameters that do not directly enter inventory calculations.

3.5.3 Workaround Strategies

When gaps cannot be immediately resolved through additional research, the following strategies are employed:

Table 3.5: Data gap workaround strategies

Strategy	Application
Proxy data	Use data from similar process/technology with adjustment
Stoichiometric	Calculate from reaction chemistry
First principles	Derive from physics (energy, mass balance)
Literature range	Use reported range from multiple sources
Expert estimate	Document assumptions and basis
Exclusion	Omit with documented justification (for minor flows)

3.6 Validation Approach

3.6.1 Internal Consistency Checks

All LCI datasets undergo internal validation with defined tolerances:

- **Mass balance**: Inputs must equal outputs plus accumulation within $\pm$5%
- **Energy balance**: Process energy must be physically plausible within $\pm$10%
- **Water balance**: Fresh water in $\approx$ wastewater out + evaporation within $\pm$10%
- **Dimensional analysis**: Units must be consistent (zero tolerance)
- **Range checks**: Values must be within physically possible bounds

Deviations beyond these tolerances require investigation and documented justification before the dataset is accepted.

3.6.2 External Benchmarking

Calculated inventories are validated against published benchmarks:

Table 3.6: Benchmark sources by component type

Component Type	Benchmark Sources
Semiconductor wafers	TSMC/Samsung sustainability reports, academic LCA
Memory	SK Hynix/Micron environmental reports
PCBs	IPC industry surveys, academic studies
Packaging	OSAT company reports, SEMI data
Passives	Academic papers, manufacturer datasheets

3.6.3 Acceptance Criteria

Validation results are interpreted as:

$<$**30% deviation** Acceptable; document any known reasons

30–100% deviation Investigate; may be acceptable with justification
>**100% deviation** Likely error; must resolve before use

For parameters with high uncertainty (yield, utilization efficiency), wider acceptance ranges may apply with documentation.

3.7 Reporting Data Quality

3.7.1 Dataset-Level Summary

Each LCI dataset includes a data quality summary:

```
Data Quality Summary: 7nm Node
----------------------------------------
Category        | Parameters | Avg DQI | High-Priority Gaps
Lithography     |     12     |   1.8   | None
Etch            |     24     |   2.3   | NF3 flow rates
Deposition      |     31     |   2.5   | ALD precursor util
Wet clean       |      8     |   3.1   | Chemical volumes
Overall         |     75     |   2.4   | 3 gaps
```

3.7.2 Flow-Level Documentation

LCI exports include per-flow quality metadata:

- DQI composite score
- Individual dimension scores
- Uncertainty range (min/typical/max)
- Source reference
- Notes on limitations or caveats

3.8 Database Quality Assessment

This section presents the data quality assessment results for the current database release, generated using the automated quality scoring system described in the preceding sections.

3.8.1 Data File Statistics

Table 3.7 summarizes the scope and completeness of the database *data files*. These files include component type definitions, process inventories, source extractions, and configuration data that together define the 204 component types described in Chapter 1.

Note: The 504 data files are distinct from the 204 component types. Data files include process inventories (188 files), source extractions (90 files), and component type definitions (204 files), plus supporting configuration files. Multiple component types may share process files, and some types support configuration options that produce multiple LCI datasets.

Table 3.7: Database data file statistics

Metric	Value
Total data files analyzed	504
Total data points	6,324
Data points with values	6,313 (99.8%)
Placeholders remaining	11 (0.2%)
LCI datasets with aggregated DQI	174

3.8.2 Quality by Component Category

The most actionable quality view is by component category, showing **aggregated DQI** calculated from the process files for each component type. Table 3.8 presents these results.

Table 3.8: Data quality indicators by component category (1=best, 5=worst)

Category	Datasets	Refs	Avg DQI	Quality
Substrates	2	5	2.63	Good
Logic Wafers	15	609	2.70	Good
Memory Wafers	8	273	2.72	Good
Passives	21	42	2.77	Good
Memory Components	6	16	2.80	Good
Specialty	20	168	2.88	Good
PCBs	19	177	3.25	Fair
Packaging	37	416	3.31	Fair
Electromechanical	4	21	3.61	Fair
Connectors	8	60	3.99	Fair
Cables	10	59	4.01	Poor
Thermal	5	5	4.04	Poor
Optoelectronics	10	68	3.61	Fair
Infrastructure	13	45	4.44	Poor
System Components	13	45	4.81	Poor

Refs indicates the number of process file references aggregated for DQI calculation. Categories with more refs have richer process flow definitions.

3.8.3 Interpretation of Quality Patterns

The quality assessment reveals systematic patterns that reflect the maturity of different component categories:

Good quality (DQI 2.6–3.0) Semiconductor wafers, memory, passives, and substrates (the core electronics components) have the best quality scores. These categories benefit from:

- Rigorous source documentation from equipment vendors (ASML, Applied Materials, Lam Research)
- Academic literature with peer-reviewed process data
- Corporate sustainability reports with verified facility metrics
- Detailed process flow definitions with hundreds of referenced steps

Fair quality (DQI 3.0–4.0) PCBs, packaging, electromechanical components, optoelectronics, and connectors have adequate sourcing with room for improvement. These categories typically have:

- Mix of vendor specifications and industry estimates
- Less detailed process flow definitions
- Some gaps filled with engineering calculations

Poor quality (DQI 4.0–5.0) Cables, thermal components, infrastructure, and system components are newer categories with:

- Process files marked as "estimated" with lower confidence
- Generic sources ("Engineering estimate") rather than specific citations
- Less mature data pipelines compared to semiconductor datasets

Chapter 4

Sector-Specific Modeling Approaches

This chapter details the modeling approaches for each component category, including technology-specific parameters, key assumptions, and calculation methods.

4.1 Semiconductor Fabrication (Front-End)

4.1.1 Technology Node Definitions

The database covers semiconductor nodes from 180nm to 3nm, classified into three technology generations (**irds2024**):

Table 4.1: Technology node classification

Class	Nodes	Architecture	Lithography
Advanced	3nm, 5nm, 7nm	GAA/FinFET	EUV + DUV immersion
Mature	10nm, 14nm, 22nm, 28nm	FinFET/Planar	DUV immersion
Legacy	40nm–180nm	Planar	DUV dry/I-line

Key differentiators by node class:

- **Transistor architecture**: Planar → FinFET → Gate-All-Around (GAA)
- **Minimum feature size**: Determines pattern complexity and mask count
- **Metal layers**: Advanced nodes require 12–15+ metal layers
- **EUV adoption**: Critical enabler for sub-7nm patterning

4.1.2 Process Flow Structure

Semiconductor fabrication follows a standard module structure comprising three main phases. Each phase contains multiple process steps that are modeled individually and aggregated to produce the total wafer inventory.

FEOL (Front-End-Of-Line): Transistor formation, including shallow trench isolation (STI), gate stack formation with high-k dielectrics and metal gates, source/drain engineering through epitaxy and ion implantation, and silicide contact formation. FEOL processes are characterized by high-temperature thermal steps and ion implantation, with significant contributions from oxidation, nitride deposition, and high-dose implants.

MOL (Middle-Of-Line): Local interconnect formation, including tungsten plug deposition for contacts and local interconnect layers that connect transistors to the first metal layer. MOL involves tungsten CVD, which consumes significant amounts of WF_6 precursor.

BEOL (Back-End-Of-Line): Global wiring using copper damascene metallization across 10–15+ metal layers, via formation between layers, low-k dielectric deposition and integration, and final passivation. BEOL dominates the total mask count and represents a substantial portion of total process steps and energy consumption.

The total process step count ranges from approximately 300 steps for legacy nodes (65nm and above) to over 1000 steps for advanced nodes (7nm and below), driven primarily by multi-patterning requirements and increased metal layer counts.

Figure 4.1 illustrates the overall flow from silicon wafer through the three fabrication phases to produce a processed wafer ready for dicing and packaging.

4.1.3 Mask Layer Complexity

Mask layer count scales significantly with technology node:

Table 4.2: Mask layer count by technology node

Node	Total Masks	EUV Masks	Multi-Patterning
3nm	85–100	25–30	SADP/SAQP
5nm	80–90	15–20	SADP/SAQP
7nm	80–85	5–10	LELE/SADP
14nm	55–60	0	LELE
28nm	40–45	0	Single
65nm	30–35	0	Single

Multi-patterning techniques:

- **LELE**: Litho-Etch-Litho-Etch (2 masks per layer)
- **SADP**: Self-Aligned Double Patterning
- **SAQP**: Self-Aligned Quadruple Patterning

Cut-off note: The fabrication of photomasks themselves is **excluded** from the system boundary based on cut-off criteria. For high-volume production, the embodied energy of the mask set is amortized across tens of thousands of wafers, contributing less than 0.1% to per-wafer inventory. For low-volume advanced ASIC production where mask cost per die is significant, users may need to add mask fabrication impacts separately.

4.1.4 Lithography Modeling

Lithography represents a significant portion of fab energy consumption:

Table 4.3: Lithography system energy profiles

System	Power (kW)	WPH	kWh/wafer	Nodes
EUV (NXE:3600)	1000	150–170	6–7	3nm, 5nm, 7nm (**asml_euv**)
DUV Immersion	80–100	250–275	0.3–0.4	All nodes
DUV Dry	40–60	150–200	0.2–0.4	28nm+
I-line	20–30	100–150	0.1–0.3	90nm+

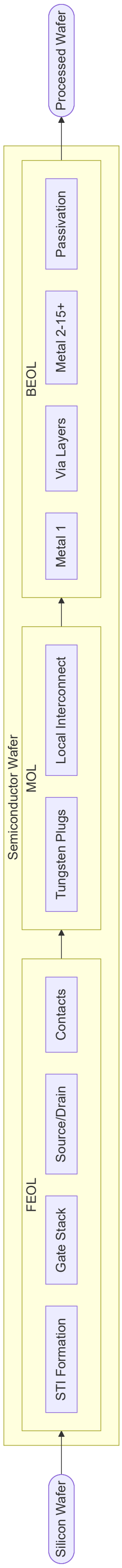

Figure 4.1: Semiconductor wafer process flow showing the three main fabrication phases: FEOL (transistor formation), MOL (local interconnect), and BEOL (global wiring). Each phase contains multiple process steps with individual inventory data.

EUV systems have multiple operating states that affect energy consumption. The active state (approximately 1000 kW) applies during wafer exposure. Between wafers and during lot changes, systems may enter standby (approximately 400 kW) or idle (approximately 200 kW) states. For inventory modeling, energy is calculated based on wafers processed per hour (WPH), which implicitly accounts for the duty cycle between active processing and other states.

4.1.5 Fab Modeling Assumptions

The virtual factory models incorporate several key assumptions about fabrication facility operations that affect how process-level inventories are aggregated and allocated.

Production Capacity Basis

Per-wafer inventory values are independent of fab production capacity; they represent the resources consumed to produce one wafer through the defined process flow. However, certain facility-level allocations (such as cleanroom HVAC and bulk gas systems) are calculated based on assumed fab characteristics:

Advanced logic (3–7nm) Reference capacity of 50,000 WSPM, consistent with reported capacities for leading-edge facilities.

Mature logic (28nm+) Reference capacity of 80,000 WSPM, reflecting higher throughput of established processes.

Memory (DRAM/NAND) Reference capacity of 100,000 WSPM, reflecting high-volume memory production.

Legacy nodes (130nm+) Reference capacity of 30,000 WSPM for 200mm wafer fabs.

Capacity utilization The models assume 100% capacity utilization, allocating all facility overhead to production output. This represents steady-state high-volume manufacturing conditions.

Equipment Operating States

Process equipment cycles through multiple operating states, each with different power consumption:

Processing Full power consumption during active wafer processing. This is the primary state used for energy calculations.

Idle Reduced power when equipment is powered on but not processing wafers. Vacuum systems, temperature control, and monitoring systems remain active.

Standby Minimum power state while maintaining readiness for rapid return to processing.

The models calculate per-wafer energy using the formula:

$$E_{\text{wafer}} = \frac{P_{\text{effective}}}{\text{WPH}_{\text{effective}}} \tag{4.1}$$

Where $P_{\text{effective}}$ is the time-weighted average power (accounting for processing, idle, and standby states) and $\text{WPH}_{\text{effective}}$ is the achieved throughput under typical production conditions. This approach implicitly captures the operating state mix for a fully utilized fab operating at 100% capacity utilization.

Cleanroom Area Allocation

Support process allocations assume standard cleanroom area requirements:

Advanced logic fabs Approximately 20,000–30,000 m^2 of ISO Class 5 or better cleanroom space for a 50,000 WSPM fab.

Memory fabs Similar or slightly smaller cleanroom footprint per wafer capacity due to more standardized process flows.

Legacy fabs Smaller cleanroom requirements per wafer due to less stringent contamination control needs.

HVAC energy is allocated proportionally based on cleanroom class requirements, with ISO Class 1–3 areas requiring significantly more air changes per hour than ISO Class 5–7 areas.

Yield Factors for Wafer-to-Die Conversion

Converting wafer-level inventory to per-die inventory requires yield factors. The database applies the following default yield assumptions:

Table 4.4: Default yield assumptions by technology maturity

Technology Maturity	Line Yield	Die Yield (100mm^2)	Notes
Mature production ($>$2 years)	95%	85–90%	High-volume, stable process
Volume production (1–2 years)	90%	75–85%	Ramping yields
Early production ($<$1 year)	80–90%	60–75%	Initial ramp, lower yields

Die yield follows the Poisson model ($Y = e^{-D_0 \times A}$) where defect density D_0 and die area A determine yield. For advanced nodes with higher defect densities or larger dies, yields decrease significantly. Users should substitute actual yield values when known, as yield is a linear multiplier on per-die inventory.

4.1.6 PFC Gas Handling

Perfluorinated compounds (PFCs) are used in etch and chamber cleaning with significant climate impact (**epa_pfc2006**). The emission calculation follows a multi-stage model:

$$E = M_{\text{in}} \times (1 - U) \times (1 - R) \times (1 - \text{DRE}) \tag{4.2}$$

Where:

M_{in} Mass of gas input (g/wafer)

U Chamber utilization (fraction reacted in process)

R Recovery rate (fraction captured for reuse)

DRE Destruction/removal efficiency of abatement

Table 4.5: PFC gas parameters

Gas	GWP	Utilization	DRE (Thermal)	DRE (Plasma)
SF_6	23,500	30%	98%	99%
NF_3	17,200	95–98%	99%	99%
CF_4	7,380	20%	86%	99%
C_2F_6	12,400	25%	98%	99%
C_4F_8	10,300	40%	98%	99%

Gas Recovery Scenarios

Three scenarios model gas recovery adoption:

No Recovery Legacy fabs (pre-2015); all unreacted gas to abatement
Moderate Recovery Industry average (2015–2020); SF_6 50%, He 60%
Best Practice Leading edge (2020+); SF_6 90%, CF_4 80%, He 95%

Bulk Gas Supply

Beyond specialty gases, semiconductor fabs consume large quantities of bulk gases (nitrogen, argon, oxygen, hydrogen, compressed dry air) for purging, inerting, and process atmospheres. The energy for bulk gas supply is included in the support process allocation (see Chapter 2) and accounts for:

- On-site cryogenic air separation units (ASU) for N_2, O_2, Ar production
- Hydrogen generation (steam methane reforming or electrolysis)
- Compression and distribution systems

For advanced logic fabs, bulk gas supply typically contributes 15–25 kWh/wafer to total support energy.

4.1.7 Water Balance

Water flows in semiconductor manufacturing are tracked in two distinct categories that require different treatment in the inventory. Following ISO 14046 terminology:

Water withdrawal Total fresh water intake from the source (gross use)
Water consumption Water not returned to the original watershed, primarily evaporative losses
Water discharge Water returned to the hydrological system after treatment (wastewater)

Fresh water withdrawal includes ultrapure water (UPW) for wafer rinsing, cleaning, and wet process chemistry, as well as process cooling water makeup. The mass balance is:

$$W_{\text{discharge}} = W_{\text{withdrawal}} - W_{\text{consumption}} \tag{4.3}$$

Consumption (evaporative losses) occurs primarily in cooling towers (approximately 15–20% of cooling water flow), exhaust scrubbers, and wafer drying processes. An evaporation factor of 20% is applied to fresh water withdrawal to estimate consumption, with the remainder becoming wastewater discharge.

Recirculated cooling water flows through closed-loop systems for tool cooling, chilled water distribution, and heat rejection. This water does not become wastewater under normal operation; only makeup water to compensate for evaporative losses and blowdown enters the fresh water balance. Recirculated cooling is tracked separately and excluded from wastewater calculations to avoid double-counting.

For process modeling, fresh water consumption is calculated from:

- UPW consumption per process step (from equipment specifications and rinse cycle counts)
- Scrubber water consumption (from abatement system specifications)
- Cooling tower makeup (from heat rejection requirements)

4.2 Packaging and Assembly (Back-End)

4.2.1 Package Type Classification

Packaging technologies are classified by interconnect method:

Table 4.6: Package type classification

Category	Types	Interconnect	Applications
Wire Bond	QFN, QFP, SOIC, BGA	Gold/copper wire	Consumer, automotive
Flip-Chip	FC-BGA, FC-CSP	Solder bumps	Processors, high-perf
Fan-Out	FOWLP, InFO	RDL + bumps	Mobile AP, RF
2.5D/3D	CoWoS, HBM, EMIB	TSV + interposer	HPC, AI accelerators

4.2.2 Die-to-Package Material Ratios

Material content varies significantly by package type:

Table 4.7: Typical material content by package type (relative to die mass)

Package	Substrate	Mold	Interconnect	Total/Die
QFN (5×5mm)	Leadframe 3×	EMC 5×	Wire 0.1×	8–10×
FC-BGA (35mm)	Organic 15×	EMC 8×	Bumps 0.5×	20–25×
FOWLP	RDL 2×	EMC 3×	Bumps 0.3×	5–7×
CoWoS	Si interposer 5×	Underfill 2×	μbumps 0.2×	8–12×

4.2.3 Wire Bonding Considerations

Wire bond material choice significantly affects inventory:

Table 4.8: Wire bonding material comparison

Wire Type	Diameter	mg/bond	Notes
Gold (Au)	20–25 μm	0.01–0.02	High reliability, high cost
Copper (Cu)	18–25 μm	0.008–0.015	Lower cost, harder process
Palladium-coated Cu	20 μm	0.01	Compromise solution
Silver (Ag)	20–25 μm	0.01–0.02	LED applications

Industry trend: Gold → copper transition reduces precious metal use by 60–80% per bond.

4.2.4 Advanced Packaging

2.5D Integration (CoWoS, EMIB)

CoWoS packaging involves multiple process steps, each contributing to the total packaging inventory:

Silicon interposer fabrication TSV etching, liner deposition, copper fill, and redistribution layer (RDL) formation using processes similar to BEOL wafer fabrication.

Microbump formation Copper pillar plating with solder cap for fine-pitch interconnect.

Die bonding Thermocompression bonding of chiplets to the interposer with high placement accuracy requirements.

Assembly completion Interposer attachment to organic substrate, followed by underfill dispensing and optional overmold encapsulation.

3D Stacking (HBM)

High Bandwidth Memory combines DRAM die fabrication with advanced 3D stacking:

TSV formation Through-silicon vias are etched and filled in DRAM dies prior to thinning, enabling vertical interconnect.

Die thinning Wafers are thinned to 50–100 μm to enable stacking while maintaining mechanical integrity.

Die stacking Multiple thinned DRAM dies (4, 8, or 12 high) are stacked using either thermocompression bonding with microbumps or direct hybrid bonding.

Stack assembly The completed DRAM stack is bonded to a base logic die and packaged.

Figure 4.2 shows a representative complete IC model, illustrating how wafer fabrication inventory is combined with packaging and test operations to produce the total component inventory.

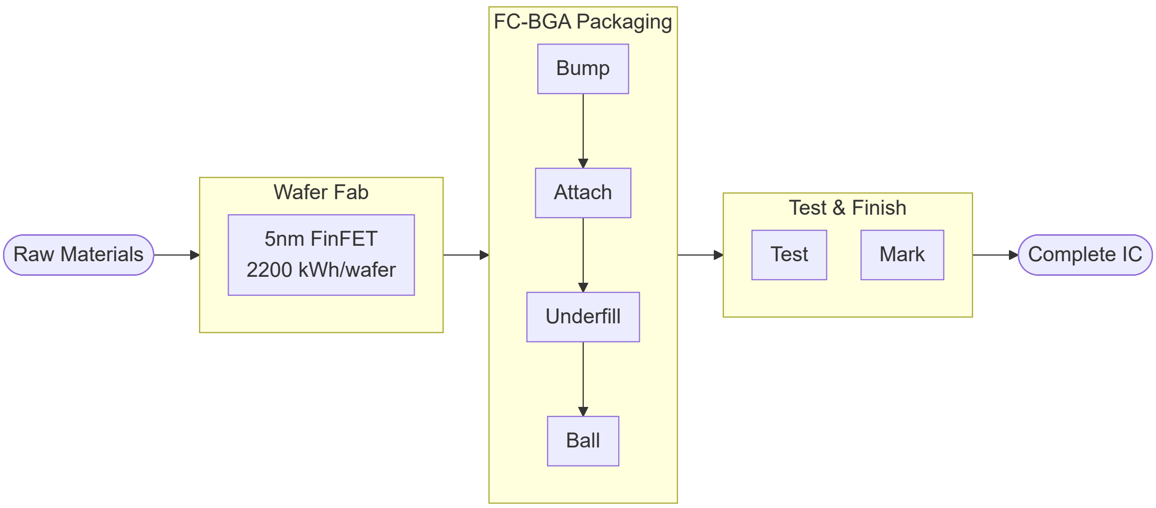

Figure 4.2: System boundary for a complete integrated circuit (5nm logic in FC-BGA package). Wafer fabrication inventory is allocated per die, then combined with packaging processes (bumping, die attach, underfill, ball attach) and final test operations.

4.3 Printed Circuit Boards

4.3.1 Layer Count Scaling

PCB complexity scales with layer count:

Table 4.9: PCB energy and water by layer count

PCB Type	Layers	kWh/m^2	L/m^2
Standard consumer	4	200–250	4000–5000
Standard industrial	6	280–350	5500–7000
Server motherboard	12–16	450–650	9000–12000
Networking/HPC	18–24	650–900	12000–16000
Backplane	28–40	900–1400	16000–25000

The major process steps contributing to PCB energy consumption, expressed as approximate percentage contributions for a typical multilayer board:

Electroplating (35–45%) Copper plating for through-holes and surface layers dominates energy consumption due to high current densities and long plating times.

Lamination (20–30%) High-temperature pressing cycles for bonding prepreg layers require significant thermal energy.

Imaging and developing (10–15%) Photoresist exposure and development, including UV lamps and conveyorized processing.

Drilling (5–10%) Mechanical drilling for vias and mounting holes; energy scales with hole count.

Etching and stripping (5–10%) Copper etching and resist stripping operations.

Surface finish and final processes (5–10%) HASL, ENIG, or other surface treatments plus final routing.

These distributions are based on process modeling from equipment specifications and are consistent with published industry surveys.

4.3.2 Surface Finish Variants

Surface finish significantly affects material and process inventory:

Table 4.10: Surface finish comparison

Finish	Thickness	Market Share	Applications
HASL (lead-free)	1–25 μm Sn	20%	Low cost, general
ENIG	3–6 μm Ni + 0.05 μm Au	35%	Fine pitch, wire bond
OSP	0.2–0.5 μm organic	30%	Cost-sensitive
ImAg	0.1–0.4 μm Ag	10%	High frequency
ImSn	0.8–1.2 μm Sn	5%	Press-fit connectors

ENIG (Electroless Nickel Immersion Gold) has highest impact due to:

- Nickel electroless plating (energy-intensive)

- Gold immersion (precious metal)
- Multiple rinse cycles

4.3.3 Panel Utilization

Manufacturing waste factors:

- **Panel edge trim**: 5–10% of panel area
- **Routing waste**: 3–8% (depends on board geometry)
- **Test coupons**: 2–5%
- **Yield loss**: 5–10% (layer-dependent)

Effective utilization: 70–85% of panel area becomes product.

4.3.4 Chemical Management

Key chemical processes:

- **Etching**: Cupric chloride or alkaline ammonia; 50–70% copper recovery
- **Electroless copper**: Formaldehyde-based reduction
- **Electroplating**: Acid copper sulfate, 85–95% current efficiency
- **Cleaning**: Alkaline cleaners, DI water rinses

4.4 Passive Components

4.4.1 MLCC Modeling

Multilayer Ceramic Capacitors (MLCCs) are modeled by size code and dielectric type.

Size Code Scaling

Table 4.11: MLCC size codes and typical parameters

Size Code	L×W (mm)	Mass (mg)	Layers	Rel. Energy
01005	0.4×0.2	0.1–0.2	50–100	0.3×
0201	0.6×0.3	0.3–0.5	100–200	0.5×
0402	1.0×0.5	1.5–2.5	200–400	1.0×
0603	1.6×0.8	5–10	300–500	1.5×
0805	2.0×1.25	15–25	400–600	2.0×
1206	3.2×1.6	50–80	500–800	3.0×

Dielectric Types

C0G/NP0 Temperature stable (Class I); lower capacitance/volume

X7R General purpose (Class II); ±15% over temperature

X5R High capacitance (Class II); ±15%, narrower temp range

Y5V Maximum capacitance; +22%/-82% variation

Sintering Process

Sintering is the dominant energy-consuming step in MLCC manufacturing, accounting for the majority of total production energy. The sintering process parameters vary by dielectric formulation:

Temperature profile Peak temperatures range from 1100 °C for Class II dielectrics (X7R, X5R) to 1350 °C for Class I (C0G/NP0), with controlled heating and cooling ramps.

Duration Total cycle times of 2–8 hours depending on part size and dielectric system, including ramp-up, soak, and controlled cooling phases.

Atmosphere Reducing atmosphere (N_2/H_2 mix) is required when using base metal (nickel) electrodes to prevent oxidation while achieving proper dielectric properties.

4.4.2 Chip Resistors

Chip resistors are fundamental passive components used in virtually all electronic circuits for current limiting, voltage division, and signal conditioning. Manufacturing processes differ significantly between thick-film and thin-film types, with corresponding differences in inventory profiles.

Thick-Film Resistors

Thick-film chip resistors represent over 90% of global chip resistor production due to their low cost and adequate performance for most applications. The manufacturing process involves multiple steps:

Substrate preparation 96% alumina (Al_2O_3) ceramic substrates are scored, cleaned, and prepared for screen printing. Substrates are typically processed in large panels that are later singulated.

Resistor printing Ruthenium oxide (RuO_2) based resistive paste is screen-printed onto substrates. The paste composition determines the base resistance value, with different formulations for different resistance ranges.

Firing Printed substrates are fired at 850 °C peak temperature in a belt furnace, typically requiring 30–60 minutes total cycle time. This step sinters the resistive material and establishes the base resistance value.

Laser trimming Resistance values are adjusted to specification by laser ablation of the resistive film. This is a critical step that determines final tolerance and represents 10–15% of manufacturing energy.

Termination End terminations (silver, nickel, or tin) are applied by printing or plating, followed by barrier and solderable layers for board attachment.

Protective coating Glass or polymer overcoat protects the resistive element from environmental degradation.

Energy consumption for thick-film resistors is dominated by firing operations (approximately 60–70% of total) and laser trimming (10–15%).

Thin-Film Resistors

Thin-film resistors serve precision applications requiring tight tolerances (±0.1% available) and low temperature coefficients. The manufacturing process uses vacuum deposition techniques borrowed from semiconductor fabrication:

Substrate High-purity alumina or silicon substrates provide stable dimensional references.

Deposition Resistive films (typically NiCr or TaN) are deposited by sputtering in vacuum chambers at 0.1–10 Pa pressure. Film thickness (50–500 nm) is precisely controlled to achieve target sheet resistance.

Patterning Photolithographic patterning and wet or dry etching define resistor geometry with high precision, enabling accurate resistance values without laser trimming for many applications.

Passivation Silicon nitride or other protective layers are deposited to prevent oxidation and ensure long-term stability.

Thin-film resistors require 3–5 times more energy per piece than thick-film equivalents due to vacuum processing requirements, but the higher precision reduces the need for binning and sorting operations.

4.4.3 Inductors

Chip inductors store energy in magnetic fields and are essential for power management, RF filtering, and signal processing applications. Manufacturing approaches differ based on required inductance values, current handling, and frequency characteristics.

Multilayer Chip Inductors

Multilayer chip inductors are fabricated using ceramic processing techniques similar to MLCCs, enabling miniaturization and high-frequency performance:

Core material Ferrite ceramics are formulated from iron oxide combined with other metal oxides. NiZn ferrites provide high resistivity suitable for frequencies above 1 MHz, while MnZn ferrites offer higher permeability for lower-frequency power applications.

Conductor formation Silver or silver-palladium paste is screen-printed in a spiral pattern on unfired ferrite sheets. Multiple sheets are stacked to create 3D coil structures with the desired number of turns.

Lamination and singulation Stacked sheets are pressed together and cut into individual parts while still in the green (unfired) state.

Co-firing Parts are sintered at 900–1000 °C in controlled atmosphere furnaces. The co-firing process simultaneously densifies the ferrite body and forms the internal silver conductors. Cycle times of 4–8 hours are typical.

Termination External electrodes are applied by dipping or printing, followed by nickel barrier and tin solderable layers.

Energy consumption is dominated by the sintering process (65–75% of total), with ferrite powder preparation and termination plating contributing the remainder.

Wire-Wound Inductors

Wire-wound inductors achieve higher inductance values and current ratings than multilayer types by using discrete wire windings around magnetic cores:

Core fabrication Ferrite cores are formed by pressing ferrite powder into drum or toroidal shapes, then sintering at 1000–1200 ℃. Core geometry determines the magnetic path length and cross-sectional area, which together with turns count set the inductance.

Winding Copper magnet wire (typically 0.02–0.2 mm diameter) is wound onto cores using automated winding machines. Turn counts range from a few turns for high-current power inductors to hundreds of turns for high-inductance signal inductors.

Termination Wire ends are welded or soldered to termination pads. Surface-mount wire-wound inductors include molded or printed external electrodes for board attachment.

Encapsulation Many wire-wound inductors receive epoxy or molded encapsulation for mechanical protection and improved thermal performance.

Core sintering represents 50–60% of total energy consumption, with winding operations contributing 15–20% and termination/encapsulation accounting for the remainder. Wire-wound inductors typically require 2–3 times more energy per piece than equivalent-size multilayer inductors due to the discrete core firing step.

4.4.4 Other Capacitor Types

Tantalum Capacitors

- Anode: Sintered tantalum powder
- Dielectric: Anodized Ta_2O_5
- Cathode: MnO_2 or polymer
- High energy due to tantalum processing

Aluminum Electrolytic

- Anode: Etched aluminum foil
- Dielectric: Anodized Al_2O_3
- Cathode: Electrolyte + aluminum foil
- Energy dominated by foil etching and forming

Film Capacitors

- Dielectric: Polypropylene (PP) or polyester (PET)
- Electrodes: Metallized film or foil
- Lower energy than ceramic/tantalum
- Larger form factor

4.5 Memory Components

Memory manufacturing shares many process steps with logic fabrication but has distinct characteristics that affect inventory modeling.

4.5.1 DRAM Wafer Fabrication

DRAM fabrication differs from logic in several important ways that affect both process complexity and per-wafer inventory:

Capacitor formation DRAM cells require high-aspect-ratio capacitor structures, either as deep trenches or tall stacks, using specialized deposition and etch processes.

Technology node naming DRAM nodes (1α, 1β, 1γ) reflect process generations rather than minimum feature sizes, making direct comparison with logic nodes misleading.

Yield characteristics The highly regular array structure of DRAM enables higher die yields compared to logic at equivalent feature sizes.

Process complexity DRAM requires fewer mask layers and process steps than logic at comparable feature sizes, resulting in lower per-wafer energy consumption.

4.5.2 3D NAND

3D NAND flash memory achieves density scaling through vertical stacking rather than lateral feature scaling, fundamentally changing the relationship between technology generation and inventory:

Vertical scaling Current production spans 128 to 300+ layers, with each generation adding layers to increase bit density.

Process challenges High-aspect-ratio etching (exceeding 50:1) and conformal deposition through deep features are critical process steps that become more demanding with increasing layer count.

Energy scaling Unlike lateral scaling in logic, vertical NAND scaling increases per-wafer energy consumption as layer counts grow. Each additional layer set adds to total deposition, etch, and inspection requirements.

Lithography requirements 3D NAND has less dependence on EUV lithography than advanced logic, as critical dimensions are not driven to the same extent by lateral pitch.

4.5.3 HBM Stacking

High Bandwidth Memory products combine DRAM wafer fabrication with advanced 3D packaging to create high-performance memory stacks. The inventory for HBM includes both the wafer fabrication component and the stacking and packaging processes:

Die structure HBM stacks consist of a base logic die (typically containing I/O and control circuitry) topped with 4, 8, or 12 DRAM dies.

TSV integration Dense through-silicon via arrays (exceeding 1000 TSVs per mm^2) provide vertical interconnection between stacked dies.

Bonding technology Either microbump bonding or direct hybrid bonding is used for die-to-die connections, with hybrid bonding offering finer pitch and better thermal performance.

4.6 Complementary Rack Infrastructure

In addition to the primary focus on semiconductor components, PCBs, and passive devices, the database includes models for **complementary rack infrastructure** to support holistic assessments of IT equipment and data center deployments.

4.6.1 Scope and Purpose

These infrastructure models cover mechanical and structural components typically found in high-performance computing racks, including:

- Server rack frames (48RU open-frame structures)
- Compute tray assemblies and slide rails
- Power distribution components (busbars, PDUs)
- Liquid cooling manifolds and interconnects
- Board pans and cable management assemblies

The models are based primarily on published industry standards, including the **OCP Open Rack V3 Base Specification** and the **NVIDIA MGX Accelerated Computing Rack and Trays Specification**. These open standards provide dimensional requirements, material recommendations (e.g., SGC400 galvanized steel for load-bearing structures), and interface specifications that enable inventory estimation.

4.6.2 Data Quality Considerations

Important: These infrastructure models represent **approximate estimates** developed without access to primary manufacturing data. Users should be aware of the following limitations:

No primary data Unlike semiconductor and PCB models which draw on equipment specifications and academic literature, rack infrastructure models rely entirely on dimensional analysis from published specifications and engineering estimates.

Mass estimation Component masses are estimated from industry benchmarks (e.g., commercial 48U rack specifications from Eaton, RackSolutions, Cheval Group) rather than direct measurement.

Material composition Material breakdowns are inferred from specification recommendations and typical data center construction practices.

Manufacturing processes Process energy is estimated using generic sheet metal forming, welding, and coating process files rather than manufacturer-specific data.

4.6.3 Intended Applications

Rack infrastructure was **not the primary focus** of the REEL LCI Database but was included to:

- Enable complete bill-of-materials coverage for IT equipment assessments
- Support **hotspot analysis** where users need to understand the relative contribution of infrastructure versus active components
- Provide order-of-magnitude estimates for **data center modelers** assessing rack-level environmental profiles

- Facilitate screening-level comparisons of different rack configurations

For applications requiring higher confidence in infrastructure impacts, users should seek manufacturer-specific data or conduct primary data collection.

4.6.4 Model Structure

Infrastructure models follow the same three-tier architecture as other component models but with simplified process flows. Material inputs are documented with ecoinvent dataset references for upstream linkage:

- Steel sheet rolling and galvanizing (for structural frames)
- Aluminum extrusion (for heat sinks and thermal components)
- Sheet metal forming and welding operations
- Powder coating for surface finishing

Manufacturing waste (blanking scrap, coating overspray) is tracked and typically represents 15–20% of gross material input for sheet metal components, with high recyclability for steel scrap.

Chapter 5

User Guidance

This chapter provides guidance for practitioners applying the REEL LCI Database in their assessments.

5.1 Integration with Background Databases

5.1.1 Upstream Material Linkage

The database provides manufacturing inventories that require linkage to upstream processes for complete cradle-to-gate assessment. Users must connect the following elementary flows to background database equivalents:

Raw Materials

Table 5.1: Key materials requiring upstream linkage

Material Class	Examples	Background Process
Silicon	Wafer substrates	Silicon wafer production
Metals (bulk)	Copper, aluminum, nickel	Metal primary/secondary production
Precious metals	Gold, silver, palladium	Precious metal refining
Specialty metals	Tantalum, tungsten, cobalt	Specific metal supply chains
Ceramics	Alumina, barium titanate	Ceramic powder production
Polymers	Epoxy, polyimide, PET	Polymer resin production
Specialty chemicals	Photoresists, solvents	Chemical production

Energy Carriers

Electricity Connect to appropriate regional grid mix (see Section 5.4)

Natural gas Link to regional natural gas supply for thermal processes

Nitrogen, oxygen, argon Link to cryogenic air separation processes

Hydrogen Link to steam methane reforming or electrolysis

Specialty gases Many specialty gases (NF_3, PFCs) may require custom supply chain modeling

5.1.2 Electricity Grid Considerations

Electricity consumption typically dominates the environmental footprint of electronics manufacturing. The database provides electricity as a separate flow to enable user selection of appropriate grid mix:

Note: Carbon intensities are approximate values for illustration and vary annually. Users should

Table 5.2: Reference electricity carbon intensities by region

Region	kg CO_2e/kWh	Production Share	Source
Taiwan	0.50	Advanced logic (TSMC)	Taiwan EPA (2023)
South Korea	0.45	Memory (Samsung, SK Hynix)	KEPCO (2023)
United States	0.40	Mixed (Intel, GF)	US EPA eGRID (2022)
European Union	0.25	Specialty, automotive	EEA (2023)
China	0.55	Growing capacity	IEA (2023)
Global average	0.45	Default assumption	IEA World Energy Outlook

obtain current emission factors from authoritative sources such as the IEA, national environmental agencies, or utility-specific data where available.

Important: Table 5.2 is provided for **screening purposes only** (quick carbon footprint estimates). For ISO-compliant LCA capturing multiple impact categories, users should link the electricity flow to a region-specific "Market for electricity" process in their background database (e.g., ecoinvent, LCA For Experts). This approach captures not only GWP but also acidification, particulate formation, and other impacts associated with the regional fuel mix.

Recommendation: Use production-weighted regional mixes when supply chain geography is known. Fall back to global average for unknown supply chains.

5.2 Allocation and Cut-off Rules

Understanding the allocation and cut-off decisions embedded in the database is essential for appropriate application.

5.2.1 Allocation Methods Applied

Facility support processes Cleanroom HVAC, UPW production, and other support systems are allocated to wafers based on production throughput (wafers per month). This assumes all wafers receive equal support burden regardless of process complexity.

Multi-product fabs For fabs producing multiple technology nodes, allocation is based on wafer throughput. Economic allocation is not used.

Yield allocation All inventory burdens are assigned to good dies; defective dies are treated as process waste with no allocation of upstream burdens.

Complete ICs Packaging and test inventories are allocated per package based on packaging yield; die inventory carries through from wafer fabrication with die yield allocation.

5.2.2 Cut-off Criteria Applied

The following are **excluded** from the system boundary based on cut-off criteria:

- Capital equipment manufacturing (cleanroom construction, process tools)
- Photomask fabrication (amortized contribution $<$0.1% per wafer for high-volume production)
- Employee transportation and facility administration
- R&D and pilot production overhead

- Ancillary materials contributing $<1\%$ of process inputs (except substances of environmental concern)

Users should consider whether these exclusions are appropriate for their specific application. For low-volume production or early-stage technologies, some excluded items may be more significant.

5.3 LCIA Method Compatibility

5.3.1 Inventory-Only Scope

This database provides **inventory data only**, not characterized impact results. Users must select an appropriate Life Cycle Impact Assessment (LCIA) method:

TRACI 2.1 US EPA method; appropriate for North American assessments
EF 3.0/3.1 European Commission Environmental Footprint; required for EU PEF studies
ReCiPe 2016 Global harmonized method; endpoint and midpoint indicators
CML-IA Widely used baseline method; midpoint indicators
IPCC GWP For greenhouse gas accounting; use AR6 values

The choice of LCIA method affects characterized results but not the underlying inventory data.

5.3.2 Elementary Flow Nomenclature

Elementary flows are mapped to ecoinvent v3.12 nomenclature for interoperability.

Compartment Structure

Emissions use ecoinvent's compartment/subcompartment hierarchy with defaults appropriate for industrial semiconductor and electronics manufacturing:

Table 5.3: Default compartment assignments for electronics manufacturing

Compartment	Default Subcompartment	Rationale
Air	non-urban air or from high stacks	Controlled point sources with abatement
Water	surface water	Treated wastewater to municipal/surface
Soil	industrial	Rare; only for direct soil emissions

Key Process Gas Emissions

Table 5.4 lists critical greenhouse gas emissions from semiconductor manufacturing with their ecoinvent mappings.

Substances Not in ecoinvent

Four semiconductor process gases are not included in ecoinvent v3.12 elementary exchanges:

- **C_4F_8** (Octafluorocyclobutane, CAS 115-25-3): Dielectric etch gas, GWP_{100} = 10,300
- **C_4F_6** (Hexafluoro-1,3-butadiene, CAS 685-63-2): Advanced etch gas
- **SiH_4** (Silane, CAS 7803-62-5): CVD precursor, pyrophoric
- **BCl_3** (Boron trichloride, CAS 10294-34-5): Metal etch gas

Table 5.4: Critical elementary flows with ecoinvent identifiers

Flow	CAS	ecoinvent Name	GWP_{100}	UUID (partial)
CF_4	75-73-0	Tetrafluoromethane	7,390	b353e7d2...
C_2F_6	76-16-4	Hexafluoroethane	12,200	8f3e0579...
SF_6	2551-62-4	Sulfur hexafluoride	22,800	c7c769bb...
NF_3	7783-54-2	Nitrogen fluoride	17,200	f8cf5fd7...
CHF_3	75-46-7	Trifluoromethane	14,800	5e2e1740...
N_2O	10024-97-2	Dinitrogen monoxide	298	afd6d670...

These flows are exported with compartment/subcompartment but without ecoinvent UUIDs. Users may need to create custom characterization factors or use proxy substances (e.g., CF_4 for fluorocarbon GWP estimation).

5.3.3 Impact Category Coverage

The inventory data supports assessment of the following impact categories:

- **Climate change**: Via electricity, fuel combustion, and direct PFC emissions
- **Acidification**: Via electricity-related SO_x and NO_x
- **Eutrophication**: Via wastewater emissions
- **Resource depletion**: Via material inputs (metals, water)
- **Photochemical oxidation**: Via VOC emissions (solvents, photoresists)
- **Human toxicity**: Via heavy metals and specialty chemicals
- **Water use**: Via fresh water consumption

5.4 Geographic Adaptation

5.4.1 Default Geographic Scope

Default geographic assumptions by component type:

Table 5.5: Default geographic assumptions by component type

Component Type	Default Geography
Advanced logic (sub-10nm)	Taiwan (TSMC dominance)
Memory (DRAM, NAND)	South Korea/Taiwan split
Mature logic (28nm+)	Global average (distributed)
OSAT packaging	China/Taiwan/Malaysia
PCBs	China/Taiwan dominant
Passive components	Asia-Pacific average

5.4.2 Regional Adaptation Procedure

To adapt data for specific supply chains:

1. **Identify actual supply chain geography** from supplier disclosures or industry knowledge
2. **Substitute electricity grid mix** with region-specific data

3. **Adjust water stress factors** if conducting water footprint analysis
4. **Consider regional efficiency variations** (documented in dataset metadata where applicable)

Example: For a product manufactured at TSMC Taiwan:

- Use Taiwan grid mix (0.50 kg CO_2e/kWh)
- Apply Taiwan water stress characterization factors
- No efficiency adjustment needed (datasets calibrated to leading-edge fabs)

Climate Adjustment Considerations

Fab location affects facility energy consumption beyond grid carbon intensity. Climate conditions influence HVAC energy requirements for cleanroom temperature and humidity control:

Hot and humid climates Fabs in tropical or subtropical regions (Taiwan, Malaysia, Singapore) require additional cooling and dehumidification energy. Support energy may be 10–15% higher than temperate baseline.

Arid climates Fabs in dry regions (Arizona, Israel) require humidification systems that consume significant water and energy, but cooling loads may be lower due to dry-bulb temperature differential.

Temperate climates Fabs in temperate regions (Oregon, Ireland, parts of Japan) have lower HVAC energy requirements and serve as the baseline for model calibration.

The REEL LCI Database uses production-weighted regional averages that implicitly account for typical climate conditions in major manufacturing regions. The default datasets assume Taiwan/Korea climate conditions for advanced logic and memory, representing the majority of global semiconductor production. Users assessing specific facilities in significantly different climates may adjust support process energy allocations by $\pm$10–15% to account for HVAC differences.

5.5 Functional Unit Selection

5.5.1 Per-Component vs. Per-Function

The database provides data per physical component unit. For functional comparisons, users must define functional equivalence:

Per component Direct use of database functional units (per die, per IC, per m^2)

Per function Requires user-defined equivalence (e.g., compute operations per second, storage capacity)

Example: Comparing processors by function:

- 7nm processor: 2000 kWh/wafer, 100 mm^2 die, 100 GFLOPS
- 14nm processor: 1200 kWh/wafer, 200 mm^2 die, 50 GFLOPS
- Per-die comparison favors 14nm (lower kWh/die)
- Per-GFLOPS comparison favors 7nm (higher efficiency)

5.5.2 Scaling to Product Level

To aggregate component inventories to product level:

1. List all components in bill of materials (BOM)
2. Match each component to appropriate LCI dataset
3. Multiply component inventory by quantity in product
4. Sum across all components
5. Add assembly and integration processes if within scope

$$I_{\text{product}} = \sum_i (I_{\text{component},i} \times Q_i) + I_{\text{assembly}} \tag{5.1}$$

5.6 Uncertainty Interpretation

5.6.1 Using Min/Typical/Max Ranges

The database provides three-point estimates (min/typical/max) for all quantitative values:

Typical value Use for point estimates and central tendency reporting
Min/max range Use for sensitivity analysis bounds
Full range Use for identifying critical parameters

5.6.2 Sensitivity Analysis Recommendations

Recommended sensitivity analysis approach:

1. **Identify dominant flows**: Focus on parameters contributing $>$10% to total impact
2. **Vary key parameters**: Use min/max bounds for dominant flows
3. **Document sensitivity**: Report how results change across the range
4. **Prioritize data improvement**: High sensitivity + high uncertainty = priority for refinement

Key parameters typically requiring sensitivity analysis:

- Electricity consumption (typically 40–60% of carbon footprint)
- Die yield (strongly affects per-die allocation)
- PFC emissions (high GWP but uncertain abatement efficiency)
- Precious metal content (high upstream impact per gram)

5.6.3 Monte Carlo Sampling

For probabilistic assessment:

1. Assume triangular distribution with min/typical/max as a/mode/b
2. Generate N samples (recommend $N \geq 1000$)
3. Propagate through calculation
4. Report median and confidence intervals (e.g., 5th/95th percentile)

5.7 Common Use Cases

5.7.1 Scope 3 Category 1 Accounting

For GHG Protocol Scope 3 Category 1 (**ghgprotocol_scope3**) (purchased goods):

1. Obtain BOM with component quantities
2. Match components to LCI datasets
3. Calculate total energy consumption (kWh)
4. Apply regional electricity emission factor to obtain electricity-related GHG emissions
5. For direct PFC emissions: sum the mass flows of each PFC gas (CF_4, C_2F_6, etc.) from the inventory and apply characterization factors from the selected LCIA method (e.g., IPCC AR6 GWP values)
6. Sum for total Scope 3 Category 1 contribution

5.7.2 Product Carbon Footprint

For ISO 14067-compliant product carbon footprints (**iso14067**):

1. Define system boundary (cradle-to-gate for manufacturing)
2. Aggregate component inventories per product BOM
3. Link electricity to appropriate grid mix
4. Apply GWP characterization factors (recommend IPCC AR6)
5. Report manufacturing footprint with uncertainty

5.7.3 Comparative Assessment

For comparing alternative designs:

1. Ensure functional equivalence is defined
2. Use consistent methodology for all alternatives
3. Compare using same LCIA method and parameters
4. Report uncertainty ranges for both alternatives
5. Conclusions valid only when ranges do not overlap significantly

Note: Per ISO 14044 (**iso14044**), comparative assertions disclosed to the public require critical review.

Chapter 6

Limitations and Future Work

This chapter documents known limitations, data gaps, and provides a framework for future improvements. Transparency about limitations is essential for appropriate use of the database.

6.1 Overall Data Quality Summary

Table 6.1 provides a summary of data quality across the major component categories using the pedigree matrix dimensions described in Chapter 3.

Table 6.1: Overall data quality indicators by component category (1=best, 5=worst)

Category	R	C	T	G	Te	DQI Avg
Semiconductor wafers (advanced)	2	2	1	2	2	1.7
Semiconductor wafers (mature)	2	2	2	2	1	1.7
Memory wafers (DRAM)	2	3	2	2	2	2.2
Memory wafers (3D NAND)	3	3	2	2	2	2.4
Packaging (wire bond)	2	2	2	3	2	2.2
Packaging (flip-chip)	2	3	2	3	2	2.4
Packaging (advanced 2.5D/3D)	3	4	2	3	3	2.9
PCBs	2	2	2	3	2	2.2
Passive components	3	3	3	3	2	2.7

Key: R=Reliability, C=Completeness, T=Temporal, G=Geographic, Te=Technological. DQI Avg is the geometric mean of the five dimensions.

The data quality patterns reflect the underlying data landscape: semiconductor wafer fabrication has the most extensive public documentation (equipment specs, academic studies, corporate disclosures), while advanced packaging and passive components have less public process-level data available.

6.2 Known Data Gaps

Data gaps are systematically tracked and prioritized based on their impact on inventory accuracy. The following sections summarize key gaps by component category.

6.2.1 Semiconductor Manufacturing

Workaround approaches:

- Generic etch recipes based on chemistry type (fluorine, chlorine, SF_6)
- Literature-based utilization factors with wide uncertainty ranges

Table 6.2: Key data gaps in semiconductor fabrication LCI datasets

Gap	Priority	Impact
Etch recipe specificity	High	Chemical consumption varies significantly by recipe
ALD precursor utilization	High	Low utilization (5–20%) means high precursor consumption
NF_3 chamber clean rates	Medium	Varies by tool and clean frequency
CMP slurry consumption	Medium	Slurry cost/impact varies by composition
Wet clean chemical volumes	Medium	Multiple rinse cycles affect total consumption
Photoresist utilization	Low	Spin coating efficiency relatively consistent

- Stoichiometric estimation for thin film precursor consumption

6.2.2 Component Packaging and Assembly

Table 6.3: Key data gaps in packaging LCI datasets

Gap	Priority	Impact
Advanced substrate materials	High	CoWoS/EMIB interposer fabrication
Underfill composition	Medium	Proprietary formulations
Thermocompression bonding energy	Medium	Tool-specific energy consumption
Mold compound variations	Low	Relatively consistent epoxy-based
Marking and serialization	Low	Minor contribution

6.2.3 Passive Components

Table 6.4: Key data gaps in passive component LCI datasets

Gap	Priority	Impact
MLCC dielectric formulations	High	$BaTiO_3$ dopant compositions proprietary
Tantalum capacitor anode	High	Tantalum powder processing varies
Sintering atmosphere details	Medium	N_2/H_2 ratio affects process
Electrode paste compositions	Medium	Nickel vs. precious metal
Termination plating details	Low	Standard Ni/Sn process

6.2.4 PCBs

6.3 Methodological Limitations

6.3.1 Virtual Factory Approach

The virtual factory modeling approach has inherent limitations:

Table 6.5: Key data gaps in PCB LCI datasets

Gap	Priority	Impact
Etchant regeneration rates	High	Copper recovery and acid reuse
HDI laser drilling energy	High	Via formation energy-intensive
Electroless copper bath life	Medium	Chemical replacement frequency
Regional efficiency variations	Medium	China vs. Taiwan vs. EU differences
Solder mask application	Low	Relatively consistent process

No measured facility data Models are constructed from equipment specifications and theoretical calculations, not actual facility measurements. Real fabs may operate differently than modeled.

Idealized process assumptions Process efficiencies represent typical or specification values, not actual operational variation. Equipment may run at different power states, utilizations, or efficiencies than modeled.

Limited process-level validation Published benchmarks are typically aggregated at the facility level (kWh/wafer, L water/wafer), making validation of individual process step estimates difficult.

Recipe simplification Actual process recipes are proprietary and highly variable. Models use generic recipes based on chemistry type rather than exact tool configurations.

6.3.2 Technology Currency

Electronics manufacturing evolves rapidly, creating technology currency challenges:

Moore's Law progression New technology nodes are introduced every 2–3 years. Models for advanced nodes (3nm, 5nm) have less validation data than mature nodes.

Equipment generation differences Equipment from different vendors and generations have varying efficiency. Models represent "typical" equipment rather than specific tool configurations.

Process recipe evolution Manufacturers continuously optimize recipes for yield and throughput. Published data may represent older process generations.

EUV maturation EUV lithography is rapidly evolving, with improving source power, throughput, and efficiency. Current models may not reflect latest improvements.

6.3.3 Geographic Representativeness

Production-weighted averages Default assumptions use production-weighted regional averages, which may not match specific supply chains.

Grid mix assumptions Electricity carbon intensity varies significantly by region and changes over time as grids decarbonize.

Facility-level variation Even within a region, facilities vary in age, efficiency, and environmental management practices.

6.3.4 Allocation Limitations

The allocation approaches used have inherent limitations that users should consider:

Facility overhead allocation Support processes (HVAC, UPW, waste treatment) are allocated uniformly per wafer based on throughput. This assumes all wafers receive equal support burden, which may not reflect actual consumption; a complex 5nm wafer may require more cleanroom conditioning than a simpler 65nm wafer.

Multi-node facility allocation When a fab produces multiple technology nodes, support is allocated by wafer count. Economic allocation (by revenue contribution) would yield different results for high-value advanced nodes.

Yield allocation timing All upstream burdens are allocated to good dies at the end of fabrication. This approach does not distinguish between early-stage failures (which could theoretically carry lower burden) and late-stage failures.

Scrap recovery credits Precious metal recovery from scrap (gold, copper) is excluded pending reliable recovery rate data. Including recovery credits would reduce net material inputs.

6.3.5 System Boundary Limitations

The following elements are excluded from the current system boundary:

Capital goods Manufacturing equipment embodied energy is not included. Fab equipment is extremely capital-intensive and may contribute significantly over equipment lifetime.

Facility construction Cleanroom construction and infrastructure are excluded. These represent significant one-time investments amortized over facility lifetime.

Wafer substrate production Silicon ingot growth and wafer slicing are treated as upstream material inputs, linked to background databases.

End-of-life Disposal, recycling, and recovery at product end-of-life are out of scope (cradle-to-gate boundary).

6.4 Appropriate Use and Cautions

6.4.1 Suitable Applications

This database is appropriate for:

- **Comparative assessments**: Comparing technology A vs. technology B using consistent methodology
- **Hotspot identification**: Identifying the most impactful components in a bill of materials
- **Screening-level LCA**: Initial assessments to guide detailed studies
- **Scenario analysis**: Understanding sensitivity to key parameters
- **Order-of-magnitude estimates**: Establishing reasonable bounds for electronics manufacturing impacts

6.4.2 Applications Requiring Caution

The following applications require additional caution:

- **Absolute environmental declarations**: Results should include uncertainty ranges and clearly state methodology limitations
- **Regulatory compliance calculations**: May require more specific or validated data
- **High-stakes procurement decisions**: Consider obtaining supplier-specific data where possible
- **Public comparative assertions**: Per ISO 14044, require external critical review

6.5 Critical Review

6.5.1 Internal Review Process

The database has undergone internal technical review including:

- Consistency checks across LCI datasets (mass balance, energy balance)
- Benchmarking against published facility intensities
- Cross-verification of data extraction from sources
- Peer review of calculation methodology

6.5.2 External Review Statement

[This section is reserved for documentation of formal external critical review. As of the current version, external critical review has not been conducted.]

Per ISO 14044 (**iso14044**), external critical review is required for:

- Comparative assertions intended for public disclosure
- Studies supporting policy decisions
- Third-party certified environmental claims

Users intending such applications should arrange appropriate critical review for their specific study.

6.6 Future Improvements

6.6.1 Priority Data Needs

High-priority improvements for future versions:

1. **ALD precursor data**: Utilization factors and consumption rates for common ALD processes
2. **Advanced packaging**: Detailed inventory for CoWoS, EMIB, and hybrid bonding processes
3. **3D NAND layer scaling**: Energy scaling with increasing layer counts (200+, 300+)
4. **EUV evolution**: Updated parameters for higher-NA EUV systems
5. **Regional variants**: Pre-calculated regional scenarios for major production geographies

6.6.2 Methodology Enhancements

Planned methodology improvements:

Enhanced uncertainty propagation Full Monte Carlo capability with correlated parameters

Dynamic temporal modeling Time-varying grid mixes and technology evolution

Capital goods inclusion Equipment embodied energy allocation when sufficient data becomes available

Automated benchmarking Systematic comparison against published industry data

6.6.3 Coverage Expansion

Planned additions to component coverage:

- Additional specialty semiconductors (GaN, SiC power devices)
- Advanced cables and interconnects
- Display components (LCD, OLED driver ICs)
- Advanced memory (next-generation HBM)
- Chiplet and heterogeneous integration packages

Appendix A

Glossary

Semiconductor Manufacturing Terms

ALD (Atomic Layer Deposition)
A thin-film deposition technique using sequential self-limiting surface reactions to achieve atomic-level thickness control.

BEOL (Back-End-Of-Line)
The portion of IC fabrication where individual devices are interconnected with metal wiring. Includes contact, via, and metal layer formation.

CMP (Chemical-Mechanical Planarization)
A polishing process combining chemical etching and mechanical abrasion to create flat wafer surfaces.

CVD (Chemical Vapor Deposition)
A deposition process where gaseous precursors react on a heated substrate to form thin films.

DUV (Deep Ultraviolet)
Lithography using 248nm (KrF) or 193nm (ArF) light sources. Includes dry and immersion variants.

EUV (Extreme Ultraviolet)
Lithography using 13.5nm light, enabling sub-7nm feature patterning with fewer masks than DUV multi-patterning.

FEOL (Front-End-Of-Line)
The portion of IC fabrication where individual transistors are formed. Includes STI, gate, and source/drain formation.

FinFET
A 3D transistor architecture with a fin-shaped channel, used at 22nm and below for improved electrostatic control.

GAA (Gate-All-Around)
A transistor architecture where the gate surrounds the channel on all sides, used at 3nm and below.

Low-k Dielectric
Insulating materials with dielectric constant below SiO_2 ($k < 3.9$), used to reduce RC delay in BEOL.

MOL (Middle-Of-Line)
The transition region between FEOL and BEOL, including local interconnects and contacts.

PFC (Perfluorocarbon)
Fluorinated gases (CF_4, C_2F_6, SF_6, NF_3) used in etching and chamber cleaning with high global warming potential.

PVD (Physical Vapor Deposition)
Deposition processes using physical mechanisms (sputtering, evaporation) rather than chemical reactions.

Reticle
The patterned mask used in lithography to project circuit patterns onto the wafer.

STI (Shallow Trench Isolation)
Isolation structures formed by etching trenches and filling with oxide to separate transistors.

UPW (Ultrapure Water)
Highly purified water (18.2 MΩ-cm resistivity) used for wafer cleaning and rinsing.

Packaging Terms

BGA (Ball Grid Array)
Package type with solder balls on the bottom surface for board attachment.

CoWoS (Chip-on-Wafer-on-Substrate)
TSMC's 2.5D packaging technology using a silicon interposer.

Flip-chip
Interconnection method where the die is flipped and bonded face-down using solder bumps.

HBM (High Bandwidth Memory)
3D-stacked DRAM using TSVs for high bandwidth memory applications.

Interposer
A substrate (silicon or organic) providing electrical connections between dies in advanced packages.

Leadframe
Metal frame providing external connections in traditional packages (QFN, SOIC).

TSV (Through-Silicon Via)
Vertical electrical connections passing through silicon dies for 3D integration.

Wire Bond
Traditional interconnection using thin wires (gold or copper) between die pads and package leads.

LCA Terms

Attributional LCA
LCA approach describing the environmentally relevant flows associated with a product system.

Cradle-to-Gate
System boundary from raw material extraction through manufacturing, excluding use and

end-of-life.

DQI (Data Quality Indicator)
Metric assessing the quality of LCI data across multiple dimensions.

Elementary Flow
Flow from or to the environment (e.g., CO_2 emission, ore extraction).

Functional Unit
Quantified performance of a product system for use as a reference unit.

GWP (Global Warming Potential)
Impact category measuring climate change contribution relative to CO_2.

LCI (Life Cycle Inventory)
Phase of LCA involving compilation of inputs and outputs of a product system.

LCIA (Life Cycle Impact Assessment)
Phase of LCA aimed at understanding environmental significance of LCI results.

Pedigree Matrix
Framework for assessing data quality across multiple dimensions (reliability, completeness, etc.).

Units and Abbreviations

kWh
Kilowatt-hour (energy)

MJ Megajoule (energy)

L Liter (volume)

kg Kilogram (mass)

g Gram (mass)

mg Milligram (mass)

sccm
Standard cubic centimeters per minute (gas flow)

slm Standard liters per minute (gas flow)

WPH
Wafers per hour (throughput)

nm Nanometer (length, technology node)

mm Millimeter (length)

μm Micrometer (length)

Appendix B

Process Inventory List

This appendix provides a comprehensive list of process inventories included in the database, organized by manufacturing category.

B.1 Semiconductor Processes

B.1.1 Lithography

Process	Description
EUV lithography	Extreme ultraviolet exposure at 13.5nm wavelength for advanced patterning
DUV immersion lithography	ArF immersion lithography at 193nm for high-resolution patterning
DUV dry lithography	ArF/KrF dry lithography for mature nodes
I-line lithography	365nm lithography for legacy and non-critical layers

Table B.1: Lithography process inventories

B.1.2 Etch

Process	Description
Silicon plasma etch	Reactive ion etching for silicon and polysilicon
Dielectric etch	Plasma etching for SiO_2 and low-k dielectrics
Metal etch	Metal layer patterning by plasma or wet etch
High aspect ratio etch	Deep contact and via etching for advanced interconnects

Table B.2: Etch process inventories

B.1.3 Deposition

Process	Description
Thermal oxidation	High-temperature oxide growth for gate and isolation
PECVD oxide	Plasma-enhanced CVD for interlayer dielectrics
PECVD nitride	Silicon nitride deposition for barriers and spacers

Process	Description
ALD high-k	Atomic layer deposition for gate dielectrics
ALD metal gate	Work function metal deposition by ALD
CVD tungsten	Chemical vapor deposition for contact fill
PVD barrier	Physical vapor deposition for diffusion barriers
PVD copper seed	Copper seed layer for electroplating
Epitaxy	Epitaxial Si/SiGe growth for strain engineering

Table B.3: Deposition process inventories

B.1.4 Planarization and Cleaning

Process	Description
Oxide CMP	Chemical mechanical polishing for dielectric planarization
Metal CMP	Copper and tungsten CMP for damascene metallization
Wet cleaning	Multi-step wet chemical cleaning sequences
Post-CMP cleaning	Slurry residue removal and surface preparation

Table B.4: CMP and cleaning process inventories

B.1.5 Other Front-End Processes

Process	Description
Ion implantation	Dopant introduction for source/drain and well formation
Rapid thermal anneal	High-temperature activation and defect annealing
Copper electroplating	Electrochemical deposition for damascene metallization
Chamber clean	In-situ chamber cleaning using NF_3 or other gases

Table B.5: Other semiconductor process inventories

B.2 Packaging Processes

Process	Description
Wafer backgrind	Wafer thinning for package integration
Wafer dicing	Die singulation by blade or laser sawing
Epoxy die attach	Die bonding using epoxy adhesive

Process	Description
Solder die attach	Die bonding using solder preform
Gold wire bonding	Interconnection using gold wire
Copper wire bonding	Interconnection using copper wire
Flip-chip bumping	Solder bump formation for flip-chip assembly
Flip-chip reflow	Solder joint formation by reflow
Underfill	Epoxy dispensing for mechanical reinforcement
Mold encapsulation	Epoxy mold compound encapsulation
Package singulation	Individual package separation
Package marking	Laser marking for identification
Final test	Electrical parametric and functional testing

Table B.6: Packaging process inventories

B.3 Advanced Packaging Processes

Process	Description
EMIB bridge placement	Embedded multi-die interconnect bridge assembly
Thermocompression bonding	Fine-pitch die bonding for 2.5D/3D integration
HBM die stacking	High bandwidth memory die stack assembly
HBM TSV stacking	Through-silicon via layer interconnection
UBM deposition	Under bump metallization for flip-chip
Solder ball placement	Ball grid array attachment
Flux application	Flux dispensing for soldering
Passivation opening	Via opening in passivation layers
Through-mold via	Vertical interconnect through mold compound
Lid attachment	Heat spreader attachment and sealing
Carrier debonding	Temporary carrier removal after processing
Burn-in test	Accelerated reliability testing

Table B.7: Advanced packaging process inventories (2.5D/3D integration)

B.4 PCB Processes

Process	Description
Inner layer processing	Imaging and etching of inner copper layers
Lamination	High-temperature pressing of multilayer stacks
Drilling	Mechanical and laser via formation
Through-hole plating	Electroless and electrolytic copper plating
Outer layer processing	Imaging and etching of outer copper layers

Process	Description
Solder mask	Protective coating application
HASL finish	Hot air solder leveling surface finish
ENIG finish	Electroless nickel/immersion gold surface finish
OSP finish	Organic solderability preservative coating
Board routing	Final board singulation
Electrical test	Continuity and isolation testing

Table B.8: PCB process inventories

B.5 Passive Component Processes

Process	Description
Ceramic tape casting	Green sheet preparation for MLCC
Electrode printing	Internal electrode screen printing
Layer lamination	Multilayer stacking and pressing
Sintering	High-temperature ceramic densification
Termination plating	External electrode formation
Thick-film resistor	Screen-printed resistive element processing
Thin-film resistor	Vacuum-deposited precision resistor processing
Inductor winding	Wire winding for magnetic components
Ferrite processing	Ferrite core sintering and preparation

Table B.9: Passive component process inventories

B.6 Thermal Management Processes

Process	Description
Heat pipe fabrication	Copper heat pipe manufacturing and charging
Vapor chamber fabrication	Two-phase thermal spreader manufacturing
Furnace brazing	High-temperature joining for thermal assemblies
Tube fabrication	Stainless steel tube forming for cooling systems
TIM preparation	Thermal interface material mixing and filling
TIM pad manufacturing	Solid thermal pad production
Heatsink extrusion	Aluminum heatsink profile extrusion

Table B.10: Thermal management process inventories

B.7 Facility Support Processes

Process	Description
Cleanroom HVAC	Air handling for cleanroom temperature and particle control
UPW production	Ultrapure water generation and distribution
Bulk gas supply	Nitrogen, argon, oxygen supply systems
Gas abatement	PFC and VOC emission treatment
Wastewater treatment	Industrial effluent treatment and discharge

Table B.11: Facility support process inventories

Appendix C

Data Sources Summary

This appendix summarizes the primary data sources used in constructing the database.

C.1 Source Categories

C.1.1 Equipment Vendor Documentation

Vendor	Coverage	Source Type
ASML	EUV/DUV lithography systems	Technical specs, sustainability reports
Applied Materials	Etch, CVD, PVD systems	Technical papers, press releases
Lam Research	Etch, deposition, CMP	Technical documentation
Tokyo Electron (TEL)	Coating, thermal processing	Equipment specifications
KLA	Metrology, inspection	Technical papers
Edwards Vacuum	Abatement systems	Product documentation

Table C.1: Equipment vendor sources

C.1.2 Academic and Research Publications

Primary sources of peer-reviewed data:

- IEEE International Electron Devices Meeting (IEDM)
- VLSI Technology Symposium
- Journal of the Electrochemical Society
- Solid State Technology
- Semiconductor Engineering

C.1.3 Industry Roadmaps

- IEEE International Roadmap for Devices and Systems (IRDS) – public portions
- SEMI Standards and technology roadmaps

C.1.4 Corporate Sustainability Reports

Manufacturing facility-level data from:

- TSMC Environmental Report

- Samsung Electronics Sustainability Report
- Intel Corporate Responsibility Report
- GlobalFoundries Environmental Reports